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BOWMAR KS-22264

TECHNICAL MANUAL

FOR

FT3 LINE TEST SET

MODEL KS-22264

Ser # 399

Bowmar

WHEN QUALITY COUNTS

Communications
Test
Equipment

Bowmar/ALI Inc.
531 Main Street
Acton, Mass. 01720

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TECHNICAL MANUAL

FOR

FT3 LINE TEST SET

MODEL KS-22264

Ser # 399

MANUFACTURED FOR WESTERN ELECTRIC

By

BOWMAR/ALI, INC.
531 Main Street
Acton, MA 01720

Revision 4
June, 1984

FT3 LINE TEST SET
TRANSMITTER
SIGNAL ERROR
10⁻⁴ERROR RATE
FAULT LOCATING
STRESS TEST
WAIT
TEST
STRESS LEVEL
REPEATER SITE
DATA OUT
RECEIVER
SIGNAL ERROR
≥10⁻⁴ERROR RATE
HISTORY
HISTORY
HISTORY RESET
FAULT LOCATING
LOOP-BACK
GOOD
BAD
SIGNAL LOSS
FRAME LOSS
DATA IN
POWER
115VAC

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1.0 INTRODUCTION

1.1 Description

The Western Electric KS-22264 FT3 Line Test Set, manufactured by Bowmar/ALI, Inc. is a portable set which provides the means to test the FT3 repeater line at the DS3 data bit rate. The set consists of a transmitter and receiver in one unit. It operates from A.C. power mains.

1.2 Scope

This manual presents instrument specifications, theory of operation, drawings and a parts list. It is intended to provide operator and technicians ready reference for use of the set and for possible troubleshooting.

1.3 Specification Summary

1.3.1 Transmitter

Data Out

Format	Non-return to zero (NRZ).
Amplitude	ECL compatible (-.8 to -1.8V) when externally terminated into 75 ohms to -2 VDC.
Data Rate	44.736 MHz to ± 20 PPM, 0 to 50°C
Scrambler	7 stage; inhibited during wait period.
Pattern	
Frame	DS3 Format
Data	Pseudo-random, 2^{15}-1 word length
Address	Modulation frequency 470 KHz ± 2% Phase modulation 70° ± 20% Modulation interval on 4 msec ± 10% Modulation interval off 4 msec ± 10% Loopback delay 500 ms ± 10%
Site Address	Two decade thumbwheel switches select address 00 to 99. Address 00 defines self test.
Stress Level	One thumbwheel switch select levels (SL) 1 to 9. Alternately forces every (10-SL) data bit to a logical "1" for 1 msec ± 10% or a logical "0" for 1 msec ± 10%.

Single Error	Momentary pushbutton inserts one parity error.
10^{-6} Error Rate	Momentary pushbutton inserts 10^{-6} ± 10% parity errors per second.
Wait Indicator	Yellow L.E.D. indicator on for 5.5 ± .5 sec. during test or stress test.
Auxiliary Outputs (Rear Panel)	
Clock Out	0 to +2 VDC ± +10% signal when terminated in 50 ohm resistive load.
Data Out	0 to +2 VDC ± 10% signal when terminated in 50 ohm resistive load.
All 0's (Rear Panel)	Momentary pushbutton switch substitutes All 0's for pseudo-random data.

1.3.2 Receiver

Data In	
Format	Non-return to zero (NRZ).
Amplitude	ECL compatible -.8 to -1.8 VDC ± 10%.
Data Rate	44.736 MHz ± 20 PPM, 0 - 50°C.
De-scrambler	7 stage; inhibited during loop-back period.
Pattern	
Frame	DS3 format Frame synchronization less than 100 msec.
Data	Pseudo-random, random, or all 0's.
History Reset	Momentary pushbutton extinguishes history indicators.
Single Error	Red L.E.D. indicator on for 25 msec ± 10% for each parity error detected.
Single Error History	Red L.E.D. indicator on for first error detected.
10^{-6} Error	Red L.E.D. indicator "ON" for 2.5 sec ± 10% for error rate equal or greater than 31 in a 2.5 sec ± 10% interval.

	10^{-6} Error History	Red L.E.D. inidcator "ON" at first error burst exceeding 10^{-6} error rate.
	Signal Loss	Red L.E.D. indicator "ON" if clock recovery is not achievable.
	Frame Loss	Red L.E.D. indicator "ON" if frame (F-BIT) or marker (M-BIT) synchronization is lost.
	Loop-Back	Red L.E.D. indicator "ON" for 5 sec ± 10% if a single 4 msec burst of phase modulation is detected.
	Good	Green L.E.D. indicator "ON" for 2 sec ± 10% during loop-back if error rate is less than 15 errors in 2 sec ± 10%.
	Bad	Red L.E.D. indicator "ON" for 2.5 sec ± 10% during loop-back if error rate is 15 or greater in 2.5 sec ± 10%.
	Auxiliary Outputs (Rear Panel)	
	Clock Out	0 to 2 VDC ± 0.3V when terminated in 50 ohm resistive load.
	Data Out	0 to 2 VDC ± 0.3V when terminated in 50 ohm resistive load.
	Error Out	0 to 2 VDC ± 0.3V when terminated in 50 ohm resistive load. One pulse per parity error greater than 5 usec.
1.3.3	Power	105 to 129 VAC, 60 Hz
1.3.4	Cables	One - AC Power Cord Two - 60 inch test cables (KS-22264 12)
1.3.5	Environment	0 to 50°C 0 to 95% relative humidity
1.3.6	Weight	23 Pounds
1.3.7	Size	Outside dimensions with cover: 7.5" H x 11" W x 11"D.

2.0 OPERATING INSTRUCTIONS

2.1 Self-Test Procedure

1. Using KS-22264 L2 test cable, connect DATA OUT to DATA IN.
2. After 2 seconds, all lamps except POWER and HISTORY should be out.
3. Set REPEATER SITE to 00 and push TEST. LOOP-BACK should come on, followed by GOOD.
4. SET REPEATER SITE to 01 and push TEST. LOOP-BACK should come on followed by BAD.
5. Set REPEATER SITE to 02 and push TEST. LOOP-BACK should not come on.
6. Set REPEATER SITE to 00 and STRESS LEVEL to 8. Push STRESS TEST. LOOP-BACK should come on, followed by GOOD.
7. Set STRESS LEVEL to 9 and push STRESS TEST. LOOP-BACK should not come on.
8. Push the HISTORY RESET switch. Both error history indicators should be off.
9. Push SINGLE ERROR. SINGLE ERROR should come on for approximately 250 ms. SINGLE ERROR HISTORY should stay on.
10. Push and hold 10^{-6} ERROR. SINGLE ERROR, 10^{-6} ERROR, and 10^{-6} ERROR HISTORY should come on.
11. Release 10^{-6} ERROR. SINGLE ERROR should go off. 10^{-6} ERROR should go off after approximately 2.5 seconds. Both history indicators should stay on.
12. Push HISTORY RESET. Both history indicators should go off.
13. Test Complete.

2.2 Fault Locating

1. Connect DATA OUT to LINE IN of 8A terminal regenerator.
2. Connect DATA IN to LINE OUT of 8A terminal regenerator.
3. Set REPEATER Site to 01 and push TEST.
4. Selected repeater site is good if LOOP-BACK comes on followed by GOOD. Ohterwise, repeater site is faulty.
5. After WAIT lamp is out, advance REPEATER SITE and push TEST. Repeat until faulty regenerator site is located.
6. If all sites test GOOD, select desired STRESS LEVEL and repeat tests using STRESS TEST instead of TEST.

2.3 Portable Signal Generator

DATA OUT provides valid signal for LINE IN of 8A regenerator or DSCR IN of TM150.

SINGLE ERROR and 10^{-6} ERROR switches insert parity errors into the transmitted data. The SINGLE ERROR switch produces one error each time this siwtch is pushed and released. A 10^{-6} error rate is inserted for as long as the 10^{-6} ERROR switch is pushed and held. Releasing this switch terminates error insertion. TEST, STRESS TEST, SITE ADDRESS, and STRESS LEVEL controls apply to fault locating tests only.

2.4 Portable Violations Monitor

DATA IN checks for parity errors in the signal from LINE OUT or REGEN MON of an 8A regenerator or from the SCR OUT of a TM150.

The SINGLE ERROR indicator comes on for each parity error detected. An error rate of 15 or more errors in 2 seconds will turn the 10^{-6} indicator on. Both indicators are equipped with history, which is reset by the HISTORY RESET switch.

SIGNAL LOSS indicates that the receiver is not able to recover clock from the data. Either no data is present or its amplitude is insufficient.

LOSS FRAME indicates the receiver's inability to recognize frame alignment (F-BITS) and/or frame marker bits (M-BITS). All error indicators will be on as the receiver does not have access to the parity bits.

LOOP-BACK, GOOD, and BAD indicators are for fault locate test only.

3.0 THEORY OF OPERATION

3.1 General

Refer to the Block Diagrams (Fig. 3.1.1 & 3.1.3) and schematics of Section 5 to correlate descriptions offered in this section.

3.1.1 Transmitter

3.1.1.1 Signal Format

The transmitter section of the FT3 Test Set is a DS-3 (FT-3) type test source. Its output consists of a continuously repeating pattern of data bits from a pseudo-random data generator (2^{15}-1 Bits) interleaved with a standard DS3 frame format, which is scrambled by a 7 stage scrambler. The output signal is compatible with the Bell System 8A Regenerator and TM150.

The single output port supplies a 44.736 MHz, non-return to zero, ECL compatible (-0.8 to -1.8V) data signal. Data is derived from a fifteen stage pseudo-random generator producing a random pattern of 32,767 bits, which is self starting. This data, in blocks of 84 bits, is inserted into a frame code consisting of frame alignment (F-BIT), frame marker (M-BIT) and control bits (C-BITS). A single master frame is composed of seven sub-frames. Each sub-frame begins with an "M" bit followed by blocks of data, C-BITS and F-BITS, as depicted in Fig. 3.1.2. Two specialized marker bits M3 and M4 contain the results of an even parity calculation over the data bits of the preceeding frame. If the sum, modulus 2 addition, of all data bits over a frame is "1", the parity bits M3, M4 are both set to "1".

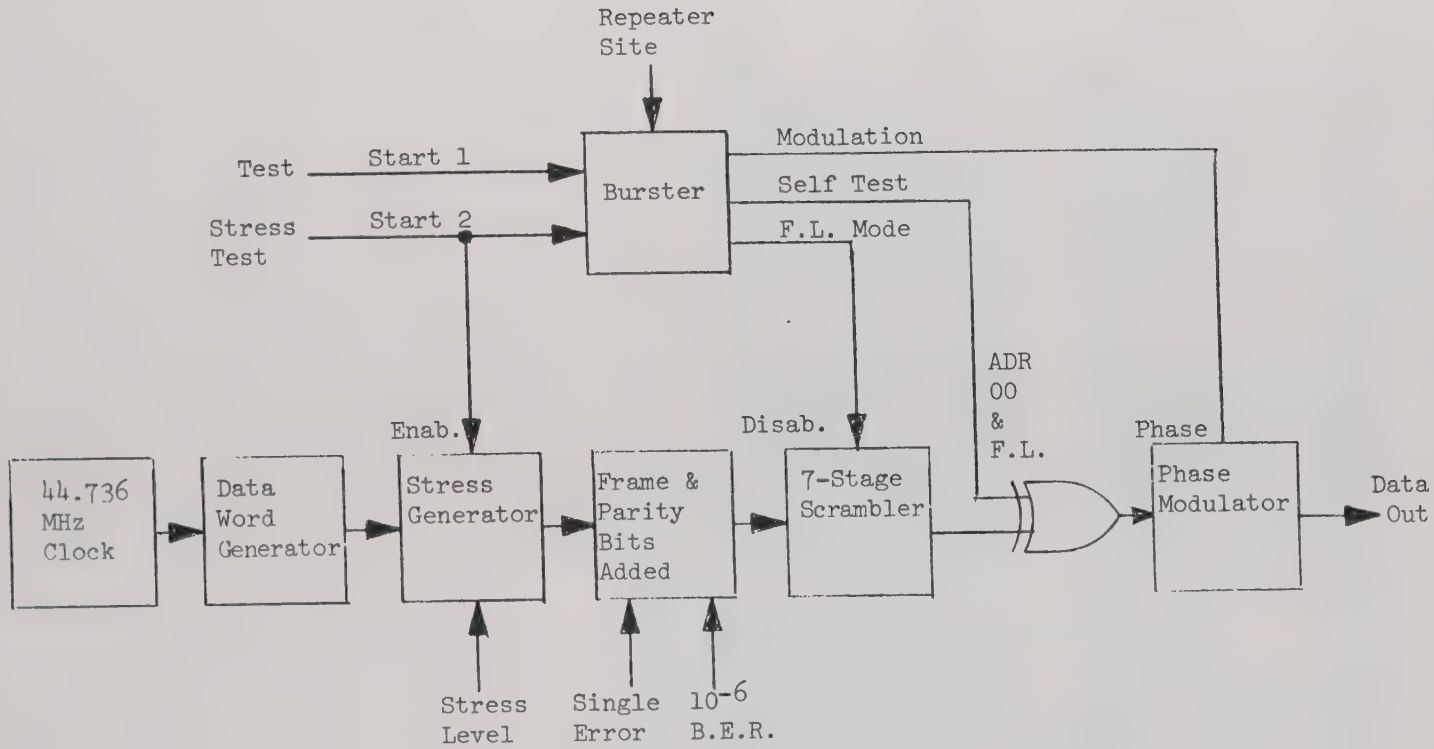

Repeater
Site
Test
Start 1
Stress
Test
Start 2
Burster
Modulation
Self Test
F.L. Mode
ADR
00
&
F.L.
Enab.
Disab.
Phase
44.736
MHz
Clock
Data
Word
Generator
Stress
Generator
Frame &
Parity
Bits
Added
7-Stage
Scrambler
Phase
Modulator
Data
Out
Stress
Level
Single
Error
10-6
B.E.R.

Figure 3.1.1

M1-84D-F1-84D-C-84D-F0-84D-C-84D-F0-84D-C-84D-F1-84D

M2	F1	C	F0	C	F0	C	F1
M3	F1	C	F0	C	F0	C	F1
M4	F1	C	F0	C	F0	C	F1
M5	F1	C	F0	C	F0	C	F1
M6	F1	C	F0	C	F0	C	F1
M7	F1	C	F0	C	F0	C	F1

M-BITS — Frame Marker
M1 = 0, M2 = 0, M3 = M4 = Parity Bits
M5 = 0, M6 = 1, M7 = 0

F-BITS — Frame Alignment
F1 = 1, F0 = 0

C-BITS — Control
All control bits in one master frame are identical with control bits in repeative frames following A 001,001,001, 001,001,011...Code.

84D — Data bits in groups of 84.

Figure 3.1.2

Parity errors may be inserted into the output data either singularly or at a 10^{-6} error rate. This is done by inverting both parity bits just prior to transmission. A single error is injected with each push of the single error switch while 10^{-6} errors are inserted as long as the 10^{-6} errors switch is pushed and held.

3.1.1.2 Loop-Back

The FT3 line regenerator has been designed with a unique addressing scheme which forces any repeater on line to LOOP-BACK. Addressing is accomplished by placing a 4 millisecond jitter burst, of 70° ± 20% peak to peak at a 470 KHz rate on the transmitted data signal. Each burst is separated by 4 milliseconds of non-jittered data. The number of burst equals the repeater site which is being requested to LOOP-BACK. Each repeater between the transmitter and the desired repeater strips off one burst. The addressed repeater recognizes that it is the one being addressed because it received only one 4 millisecond burst.

The Test Set's transmitter sends the repeater address corresponding to the Site Address (N) set on two thumbwheel switches each time the TEST or STRESS TEST switch is pushed and WAIT indicator is off. After waiting 500 milliseconds, the transmitter sends two additional addresses

sequentially plus one burst (2N+1). The addressed repeater (N) loops-back, which takes a few hundred milliseconds. This occurs during the 500 millisecond pause. During the next two address transmissions each repeater out strips off one burst and each repeater back from the one addressed strips off one burst (2N). The Test Set receives the added burst which indicates that the loop-back was successful. This is a fault locate mode operation.

Site address "00" is reserved for self test. The transmitter and receiver are connected by a test cable. When a repeater loops-back, it inverts the data. To simulate this, the transmitter inverts the data out signal for self test purposes only.

3.1.1.3 Stress Test

During stress testing the pseudo-random data is altered by the stress level switch, to either a zero or logical one. The range of the stress level (SL) control is 1 to 9. A stress level of 1 forces every 9th (10-SL) data bit to either a logical "1" for 1 millisecond or a logical "0" for 1 millisecond alternately, at a 500 Hz rate. This is the least stressful rate. At level 8 every other data bit is stressed. At level 9 all data bits are forced atlernately to a logical "0" or "1" at the 500 Hz rate. This test is initiated by the STRESS TEST switch.

3.1.2 Receiver

3.1.2.1 Clock Recovery

Data received from the system under test is processed by the receiver to determine error performance and loop-back integrity. The receiver accepts data at ECL levels (-.8 to -1.8V).

Timing is extracted from the data using a single LSI integrated circuit phaselock loop (PLL). The PLL generates a receiver clock, a phase error signal for burst detection and determines the loss signal condition.

3.1.2.2 Loop-Back

A burst detector in conjunction with a fault locating counter monitor the data for a single 4 msec phase modulation burst which defines loop-back. Once loop-back is defined, an error counter decides its good/bad quality. A good indication is registered if less than 15 parity errors occur in a 2 sec interval. Bad is defined as 15 or more errors in the same interval.

A pause of 200 msec is inserted between the detection of loop-back and the 2 sec error count interval to permit enough time for re-framing. The loop-back indicator is lighted first followed 2.2 sec later by either a good or bad indicator. The good/bad indication is on for 2 sec. The whole fault locating process takes approximately 5 sec.

The received data is sampled by the receiver clock and passed through a 7 stage de-scrambler and inverter. The received data is inverted only during the fault locate mode to make up for the data inversion introduced by the line repeater when it loops-back. This mode also disables the de-scrambler.

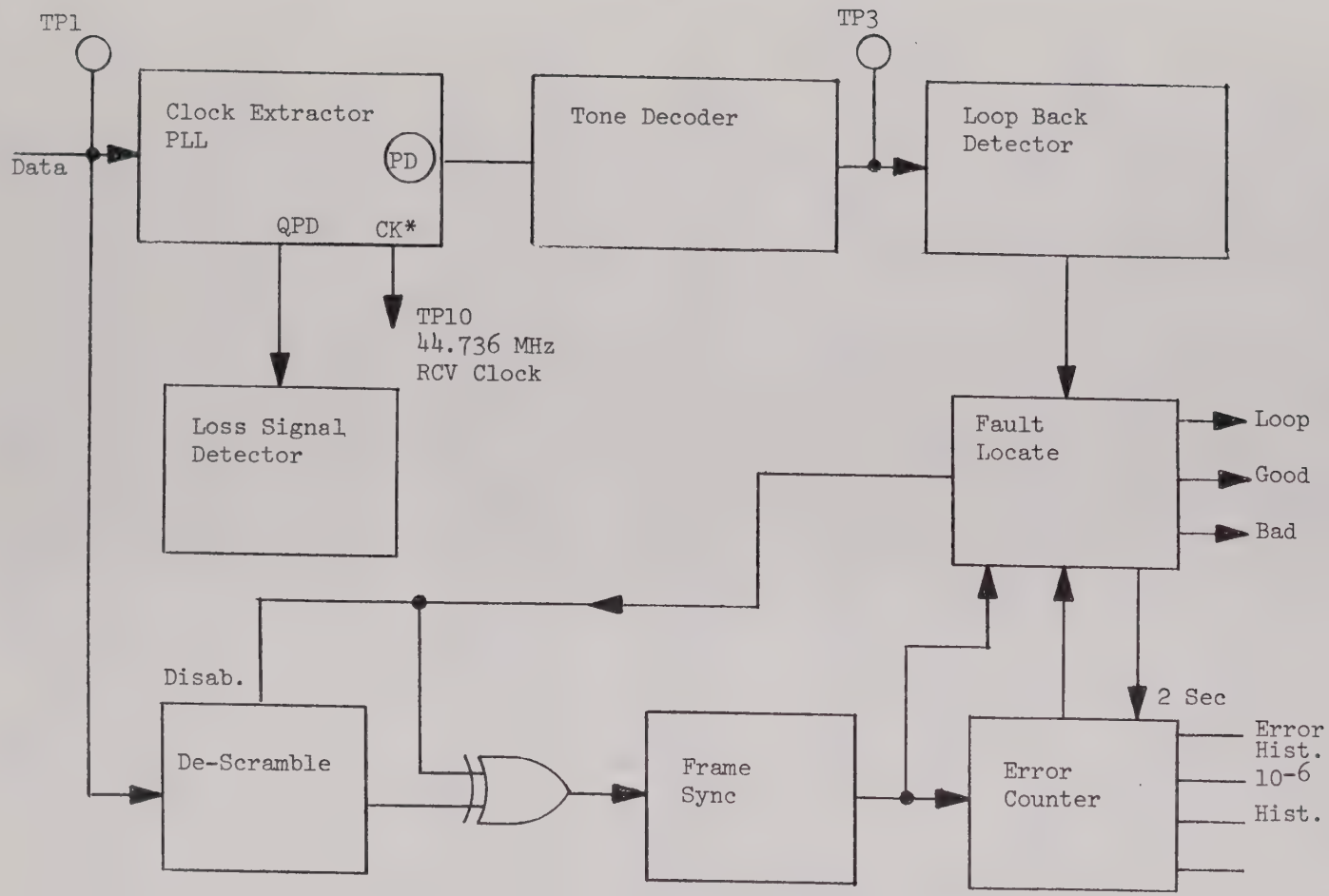

TP1
TP3
Clock Extractor
PLL
PD
Data
QPD
CK*
Tone Decoder
Loop Back
Detector
TP10
44.736 MHz
RCV Clock
Loss Signal
Detector
Fault
Locate
Loop
Good
Bad
Disab.
2 Sec
De-Scramble
Frame
Sync
Error
Counter
Error
Hist.
10-6
Hist.

Figure 3.1.3

Data is passed from the inverter to the frame recovery section. Frame synchronization, recovery, makes it possible to separate the pseudo-random data bits from the frame code bits. Frame alignment (F-BIT) and frame marker (M-BIT) must be identified within the received data bits to establish synchronization. Frame alignment is acquired first. The F-BITS consist of a 11001100... bit pattern buried within the data. A search of the data is made until 15 consecutive F-BITS are found in correct sequence and time slot position (See Fig. 3.1.2). The receiver will declare itself out of sync when 3 out of 15 bits are found incorrect. Once F-frame is found, the receiver will search for M-frame and declare itself In-frame when two successive 010 (M5, M6, M7) sequences are found. The receiver will go out of frame when two out of three 010 M-BIT patterns are bad. Either lack of F-frame or M-frame synchronization will turn on the frame loss indicator and initiate a new search. Time to acquire frame synchronization is less than 100 msec.

Sometimes it is possible to find a false F-BIT pattern in the received data. As a result M-BIT synchronization would never be found. To avoid this problem circuitry is added that requires the acquisition of M-BIT synchronization within 15 frame times after F-BIT synchronization is acquired. If M-synchronization is not reached, a "kicker circuit" pushes the receiver out of F-BIT synchronization forcing it to restart its search.

Once frame is acquired it is possible to identify parity bits (M3, M4). The parity bits are compared with a parity calculation made on all pseudo-random data bits (84D) of the preceeding frame. Any discrepancies are defined as parity errors.

Parity errors are passed to the error rate counter to determine if their frequency exceeds a 10^{-6} error rate threshold. The 10^{-6} error rate is defined as 31 or more errors in 2 seconds. Exceeding this threshold turns the 10^{-6} error indicator on for 2.5 sec. Each error detected turns on the single error indicator for 250 msec. Both functions are equipped with history indicators which are reset by the history reset switch.

3.2 Transmitter Circuits

3.2.1 44.736 MHz Clock (Fig. 5-3)

The 44.736 MHz clock is generated by a grounded base, over tone, crystal oscillator circuit. Transistor Q6 forms the basic grounded base oscillator configuration with Q4, 5 establishing an isolation amplifier function. The series capacitor C13 compensates for phase difference introduced by the tolerances of the transistors Q4, 5, 6. Capacitor C14 in conjunction with L2 form a tank circuit which is tuned to the overtone frequency of 44.736 MHz. Series capacitor C15 provides a calibration adjustment which is set for a clock frequency of 44.736 MHz $\pm$ 100 Hz.

The 44.736 MHz clock is picked off the oscillator circuit at the collector of Q4. Line receiver U18a amplifies this sinusoidal signal. The inverting input of U18a is connected to a voltage divider network consisting of R65, 66, 67. Trim resistor R66 is adjusted to produce a 50% duty cycle clock at the output of U18a.

3.2.2 Data Word Generator (Fig. 5-3)

The pseudo-random data pattern is derived from a 15-stage shift register (U30, 32, 33) whose feedback is taken from stages 14 and 15. This feedback is directed through exclusive-or gate U22a.

The Generator provides a continuously repeating sequence of 1's and 0's. Each sequence is made up of all but one of the possible 2^{15} combinations of the 15-stage shift register, for a total of 32,767 bits. The one exception is the all-zero state in which the Generator will not function. When this state does occur it is eliminated by a self start circuit (U26, U22c).

The self start circuit effectively counts the number of consecutive zeroes in the 15-stage shift register. A count of 15 or more inverts the feedback from U22a through exclusive-or gate U22c. This forces a logical "1" into the first shift register stage breaking the illegal all 0's pattern.

The Data Word Generator is driven by a gapped clock. This clock consists of the 44.736 MHz clock with a pause every 85th pulse (Sec. 3.2.5.1). As a result, blocks of 84 data bits are formed. The pause period will be filled later with a framing code bit.

3.2.3 Stress Generator (Fig. 5-3)

The Stress Generator alternately forces selected data bits to either logical "1" for 1 msec or logical "0's" for 1 msec.

Data from the Word Generator is sampled with the gapped clock by U21a. Steering logic (U24) selects either sampled data from U21a or a 500 Hz clock signal. The steering is controlled by counter U29. The combined data/clock signal is sampled by U21b which interfaces with the control bit data generator and parity generator.

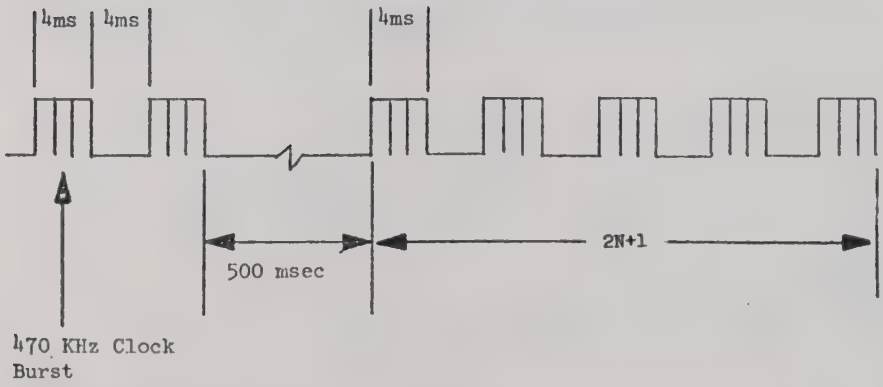
The 500 Hz clock is a logical "1" for 1 msec and a "0" for 1 msec. This signal determines the logical level of the displaced data bit during stress testing.

The stress level is determined by the Stress Level Thumbwheel switch. A stress level of one forces a displacement of every 9th data bit. This is achieved by pre-loading the decade counter U29 with the BCD equivalent of the stress level through the interface circuit U28. The counter steps to state nine, at the bit rate, and synchronously pre-sets itself to the selected stress level. This results in an effective calculation of ten minus the stress level setting. Stress level 9 selects the 500 Hz clock generator only, displacing all data bits. The stress test is initiated by the stress test switch which removes the reset on U29 for 5 seconds.

The clear input of U21a is connected to the All 0's circuit through CR3, R90, 92 which form a level translation to ECL. Pressing the All 0's switch clears U21a preventing pseudo-random data to pass and setting the data level to a logical "0". Note that U21a Pin 3 consists of inverted data.

3.2.4 Address Generator (Fig. 5-5)

The repeater site addressing code is produced by the Address Generator. A site address is converted into 470 KHz clock bursts lasting 4 msec separated by 4 msec of no clock. An address defined as "N" selected by the Repeater Site switches, is transmitted as N, 4 msec clock bursts followed by a 500 msec wait followed by 2N+1, 4 msec bursts. The following diagram illustrates the case for N=2.



n = 2

A sequence counter (U29) controls two binary counters (U18, 24) which convert the selected site address into 4 msec pulses. The Address Generator is at rest when the sequence counter is reset to state 000. The two binary counters (U18, 24) are continuously preset with the site address BCD code from the two Site Address switches. These preset inputs reach the counters through multiplexers (U17, 22) and interface circuits (U16, 21).

A special case exists for address "00", self test. During self test the output data is inverted and a single 4 msec jitter burst is transmitted. Binary counters U18, 24 are pre-loaded with a 1111 code which forces the ripple carry output of U24 to a logical "1". NAND gate U19a decodes the "00" address state if it receives a ripple carry output when the sequence generator (U29) is in the rest state. The decoding of address "00" inhibits the sequency generator (U29) from counting by application of a "0" input to NAND gate U27a. The single 4 msec output pulse is generated by U28b and transmitted through U23c to modulating gate U25b. This modulating gate combines the 470 KHz clock with a 125 Hz clock, which determines the 4 msec burst period, and outputs from the address counter (U18, 24) or Self Test decoder.

Addresses above zero are produced by Binary Counter U18, 24 under the control of the sequence generator. The sequence generator is pushed out of state 000 to state 001 whenever the Test or Stress Test switch is pushed, if the Wait indicator is off and address 00 is not selected (U28). Sequence state 001 permits the binary counter to count up from the complemented input address, established during state 000, at a 125 Hz rate. Binary counter U18 will be required to count as if it were a decade counter if the selected address is greater than ten. This transformation is executed by presetting U18 with a binary six each time it overflows count fifteen. The preset number six is selected by multiplexer U17. The sequence counter U29 is pushed into the second state (010) when the most significant binary counter U24 overflows. Stage 001 lasts for 8 msec times the address selected. During this time N, 470 KHz clock bursts, are generated corresponding to the site address.

The Binary Counters are loaded with the number 96 at the beginning of sequence state 010, selected by multiplexers U17, 22. It requires 61 pulses of the 125 Hz clock to overflow the Binary Counter U24. This corresponds to approximately 500 ms $\pm$ 10%, the second part of the transmitted address code. Bursts are not transmitted during this time.

The complement of the site address is loaded into the Binary Counters at the beginning of state 011. When the counters overflow, state 100 is reached presetting the counter again to the complement of the site address. This preset operation requires 8 msec which produces one 4 ms burst. State 011 therefore, produces N+1 bursts with state 100 producing N bursts. The result being the last part of the address code 2N+1. The end of state 100 pushes the sequence counter to its rest position state 000.

3.2.5 Frame And Parity (Fig. 5-3)

The Frame and Parity circuits are responsible for generating the frame code (F,M,C Bits), parity calculation, parity errors, the 125 Hz plus 500 Hz clock and interleaving data from the pseudo-random generator with frame bits. Consulting the expanded block diagram for these functions, Fig. 3.2.5 and Frame Code diagram, Fig. 3.1.2. will be helpful.

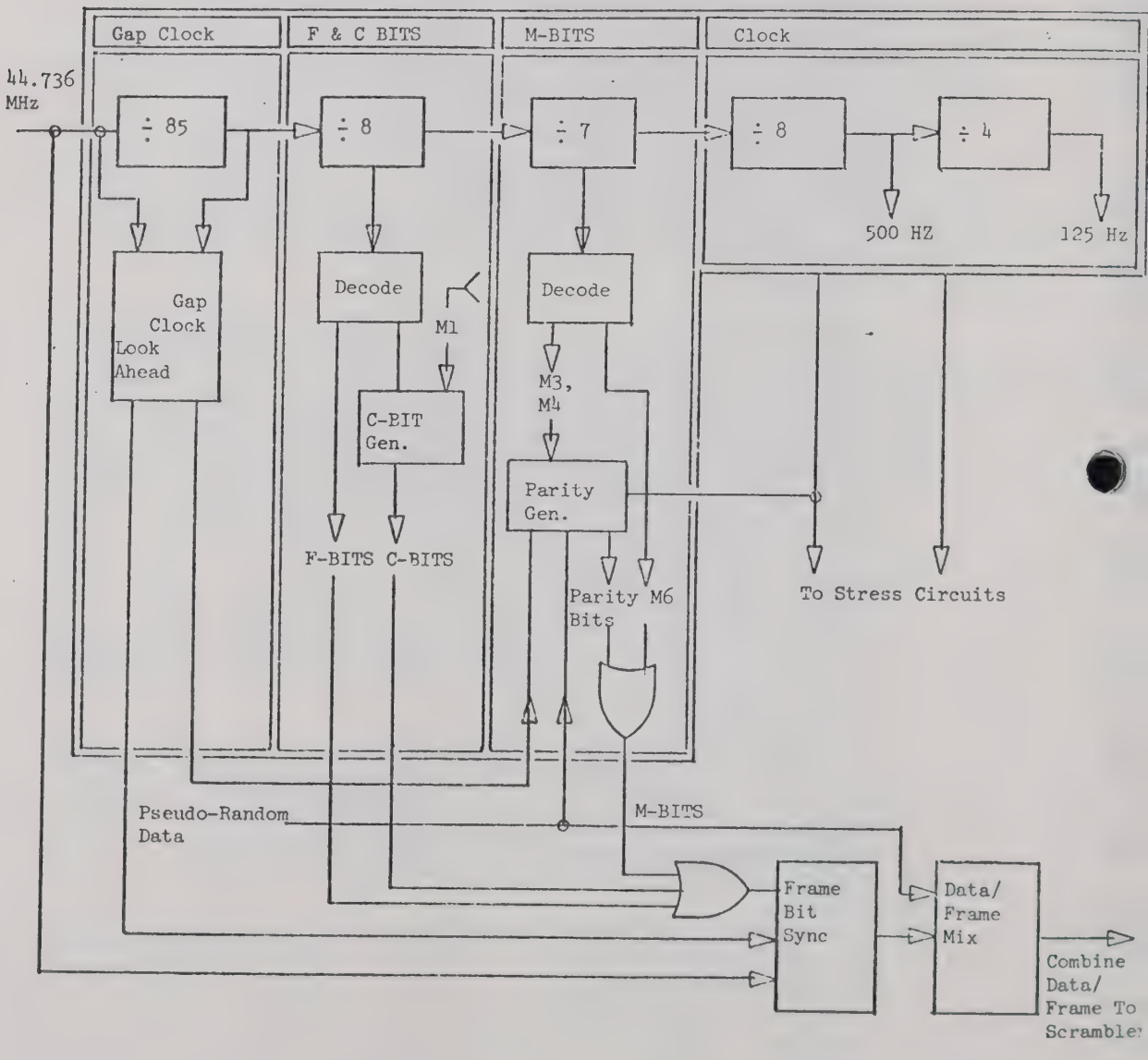


Fig. 3.2.5

Frame & Parity Block Diagram

3.2.5.1 Gap Clock (Fig. 5-3)

Framing bits are separated by 84 pseudo-random data bits. The pseudo-random data generator is inhibited during the frame bit time. This inhibit is asserted by deleting one clock edge, forming the Gap Clock.

A divide by 85 counter is formed from U2, 7, 6d. An output from this counter in conjunction with U5a, 9b, 3a produce the Gap Clock. A by-product of this process forms a look-ahead pulse (U9b). The look-ahead occurs one-half data bit before the occurence of a frame bit and aids in the interleaving of data and frame bits.

3.2.5.2 Frame Alignment & Control Bits (Fig. 5-3)

Each frame consists of seven subframes. A subframe consists of eight frame bits spaced at 85 time slot intervals, one M-Bit, four F-Bits, and three C-Bits. The logical value (1 or 0) of the "F" and "C" bits and their time position within the subframe are determined by this circuitry. The F and C bits in each of the seven subframes are identical. The value of the C-Bits change from frame to frame following a 001001001001001011 code (18 frames per super frame).

A divide by eight counter (U13) divides the output of the Gap Clock circuit producing the time sequence of the subfame bits. The F Bits are decoded by the gate combination of U4b, 10c, 4a. Since all frame bits will be ORed together at a later time is is necessary to decode only those which are defined as logical 1's, the rest will automatically become "0's". The C-Bits are decoded by gates U8b, 4c. An input to U8b (Pin 13) determines the logical level of these bits as defined by an output of the C-Bit generator.

The C-Bit code (Fig. 5-5) is formed by Shift Register U6 whose output ($\overline{Q}$) is fed back by exclusive-OR gate U9. NAND gate U7b prevents the occurence of an illegal state. The shift register produces a continuous 001 pattern. The complete C-Bit pattern is combined by U7c which adds a logical "1" to every 6th 001 group forming a 001 group. The added "1" is generated by counter U13 ($\div$ 6) and U7a.

3.2.5.3 Frame Marker Bits (Fig. 5-3)

The Frame Marker Bits consist of the first bit in each subframe in a 0,0,P,P,0,1,0 sequence. The two PP Bits (M3, 4) are designated parity bits and equal the mathematical result of adding all pseudo-random data bits in the preceeding frame. This calculation is preformed by the parity generator. The last three bits (M5, M6, M7) are used by the receiver to acquire marker synchronization, thus identifing the time position of each subframe.

A divide by seven counter (U15) provides timing information for each of the seven M-Bits. The M-6 bit is decoded by U11a, 10a, 10b. Parity bit time slots (M3, 4) are decoded by U11b, U16c.

A divide by 18 (U4, 10a) (Fig. 5-5) circuit followed by a divide by 4 (U11) create the 500 Hz $\pm$ 10% and 125 Hz $\pm$ 10% clocks from the M1-Bit. These clocks are used by the stresser, site address and parity generator circuits.

The parity calculation (Fig. 5-3) is performed between the occurence of successive M1-Bits which mark the beginning of each frame. A D-Type Flip-flop (U25b) holds the accumulated sum of each module-2 addition. Its output is connected back to the D-input through exclusive-OR gate U22b.

This gate adds the next data bit to the existing total at each positive edge of the data clock, (Gap-Clock) resulting in a summation of the pseudo-random data bits only. The result of this running sum is captured by U25a at each occurance on an M1-Bit. The running sum contains the sum of all pseudo-random data bits over the last frame plus the sum of the previous frame. Exclusive-OR gate U16a adds the output of U25b (the current sum plus the previous sum) with the inverted output of U25a which contains the result of the previous sum. The whole thing is sampled by U5 whose output represents only the sum of all pseudo-random data bits over the last frame. This operation effectively subtracts out the previous sum ambiquity. The output of U5 is gated (U3B) by the parity bit decoder positioning the parity information in the correct M-Bit (M3, 4) time slots. This signal is added to the M6 period by U3c and passed to the frame bit synchronizer.

Parity errors are inserted into the transmitted data by inverting the output of U25a, using exclusive-OR gate U16c. This in effect inverts parity bits M3 and M4, resulting in a parity error.

Parity error insertion (Fig. 5-5) is controlled by U15 which synchronizes either single error or 10^{-6} error rates to the start of a frame sequence at the occurance of M1. Single error insertion is executed by setting U15a by a signal from the Single Error switch through U5a. The 10^{-6} error pulses are established by dividing the 500 Hz clock by eleven (U12) as long as 10^{-6} Error switch is pushed and held. The ripple output of U12 is passed through U5 to trigger U15a. The error insert output of U15b is level translated to ECL by U2c and passed to exclusive-OR U16c which inverts the parity bits for that frame.

3.2.5.4 Frame Bit Synchronizer (Fig. 5-3)

All the associated frame bits are OR-ed together by U23A. These signals, due to different integrated circuit propagation delays, arrive at U23 at different times requiring the need for synchronization to the 44.736 MHz clock before the pseudo-random data can be added. The look-ahead pulse generated by the Gap Clock circuit marks the frame bit position in time, one half time slot before it must be sampled by the 44.736 MHz clock. The look-ahead clocks Flip-flop U27a which provides frame information to the data/frame multiplexer.

3.2.5.5 Data/Frame Multiplexer (Fig. 5-3)

This circuit effectively adds the output of the pseduo-random word generator with the frame bit code. The pseudo-random data at this point has passed through the stress generator.

The D-type flip-flops U27a & b accept the look-ahead pulse and synchronize it to the 44.736 MHz clock. This produces a properly positioned control signal at the outputs of U31b which steers data through U6a and frame

bits through U6b. The outputs of these gates are wire-ORed which logically adds them. This output is sampled by U31a whose output consists of data mixed with frame bits precisely aligned with the 44.736 MHz clock.

3.2.6 Scrambler (Fig. 5-3)

The scrambler consists of a seven stage shift register (U17, 12a) whose 4th and 7th stages are exclusively-ORed by U14a. A second exclusive-OR gate (U14c) mixes data from the Data/Frame multiplexer with the output of U14a. The output of U14c is defined as scrambled data. Mathematically, the scrambled data is equal to the logical exclusive-OR of the input with the 4th and 7th stage (eq 1).

$$A_m = (B_m + A_{m-4} + A_{m-7}) \quad \text{eq 1}$$

A_m = The M_{th} scrambled data bit
B_m = The M_{th} un-scrambled input data bit
A_{m-4} = A_m delayed by 4 bits
A_{m-7} = A_m delayed by 7 bits

The scrambled data is passed through exclusive-OR gate U14b to the phase modulator. This gate inverts data during the fault locate mode if address "00", Self Test, is selected. The scrambler is disabled during fault locate by an input to gate U1 which interrupts the feedback path.

3.2.7 Phase Modulator (Fig. 5-3)

The phase modulator adds jitter to the transmitted data for purpose of addressing the individual line regenerators resulting in their loopback. Jitter is added to the signal by changing the effective switching threshold of the data sampling flip-flop, U12b. In the un-modulated case a 1.5V p-p $\pm$ 20% sinusoid at the 44.736 MHz rate clocks data into the flip-flop (U12b). Addressing causes the base line of this sinusoid to oscillate at 470 KHz with a peak to peak excursion of 1V $\pm$ 20%. The level shift from standard TTL to the $\pm$ 1V signal is accomplished by transistor Q1. This base line wander occurs at each transition of the 470 KHz clock. As a result, a data bit corresponding to the 470 KHz clock transition, is sampled just before or after the position which would have resulted if the modulation were not present. The jitter added in this process has a peak to peak amplitude of 70° $\pm$ 20% (4.3 ns P_P $\pm$ 20%).

3.2.8 470 KHz Oscillator (Fig. 5-5)

The oscillator consists of a 1.88 MHz crystal (X1) and three inverters U16d, e, f. Resistor R27 controls crystal drive current. Capacitors C3 and C4 provide the crystal's capacitive load. The oscillator's output at U16d is buffered by U16c. Flip-flops U26a and b form a divide by four Johnson counter which provides the 470 KHz clock at Test Point TP2.

3.2.9 Auxiliary Outputs (Fig. 5-3)

Two of the Test Set's five auxiliary outputs (rear panel) are generated by the transmitter circuits. These include Clock Out and Data Out. Each output is connected through a line driver. Both line drivers are identical consiting of a level translator (ECL to TTL) and a transistor amplifier.

Clock Out is serviced by U19a and Q2, Data Out by U19b and Q3.

3.3 Receiver Circuits (Fig. 5-7)

3.3.1 Clock Extractor (Sheet 1)

The receiver 44.736 MHz clock, which provides timing for the receiver circuits, is generated by the Phaselock Loop (PLL) circuit U4. The phaselock loop contains a Voltage Controlled Oscillator (VCO) Phase Detectors (PD) and a Frequency Difference Detector (FDD). These components enable the PPL to phase and frequency lock its VCO to the received data. The VCO's output provides the 44.736 MHz receiver clock signal.

The Phase Detector output signal (Pin 19) is a beat note which represents the frequency difference between the data received and the VCO output. This capability is used to detect the presence of address bursts within the received data. A 470 KHz frequency component is present at this output for the duration of an address burst (4 msec). The Tone Decoder circuit (U5) uses this output to detect the address burst.

A second phase detector, Quadrature Phase Detector (QPD), determines the presence of absence of the received data signal. If data is present, the QPD output (Pin 16) is greater than -0.2V. This output is used by the signal loss detector.

The receiver clock signal is taken from an output of the VCO. The nominal frequency of the VCO is determined by the tank circuit C14 and L1. Outputs of the FDD and PD circuits are combined, amplified and connected to the VCO input representing an error correcting signal which forces the VCO to phase lock to the random received data. Resistors R14 and R15 control the loop gain. Four outputs are available: CK, $\overline{CK}$ and CK*, $\overline{CK}$*. The CK and CK* outputs are identical but are separated by a 90° phase lag. The barred outputs ($\overline{CK}$ and $\overline{CK}$*) are inversions of the CK and CK* outputs. Line receivers U1a and U7c provide the necessary interface to the remainder of the receiver circuits.

Data presented to the front panel Data In jack is passed through a line receiver (U6) (Fig. 5-1) located on the display p.c. board and differentially transmitted to the receiver board. Line receiver U1b converts the data back to base band for use by PLL and other receiver circuits. An LC filter consisting of C1 and C91 process the data before it is used by the PLL. This processing produces a signal shape similar to that of an analog channel for which the PLL was designed.

3.3.2 Loss Signal Detector (Sheet 1)

A DC voltage at the QPD output of the Clock Extractor defines the signal loss condition whenever this output is greater than -02.V. Transistor Q1 provides an interface between the U6 and U5e (LED Driver) (Fig. 5-1). The signal loss condition is displayed on the front panel by lighting the Signal Loss Indicator.

3.3.3 Tone Decoder (Sheet 1)

The Tone Decoder detects the presence of the 4 msec address bursts. The Phase Detector output of the PLL contains a 470 KHz frequency component whenever the address burst is present in the data. This signal is amplified and band pass filtered by amplifier U7a.

The heart of the Tone Decoder is a special phaselock loop (U5) intended for use as a tone decoder. Tank circuit components C9 and C10 set free run frequency of an internal Current Controlled Oscillator. Two capacitors, C17 and C18 control on/off capture delays respectively.

The Tone Decoder acquires lock whenever the 470 KHz signal is present resulting in a -5 volt level at this output (Pin 8). The width of the output pulse is approximately equal to the length of the address burst period of 4 msec. Therefore, each 4 msec burst produces one corresponding pulse.

3.3.4 Loopback Detector (Sheet 4)

Loopback is achieved when a single 4 msec address burst is detected. within a 14 msec period. The 14 msec period is determined by a digital one-shot centered about binary counter U59. Outputs of the Tone Decoder and Loss Signal circuits are AND-ed together by U46 and clock flip-flop U55a. Flip-flops U55a + b synchronize this combined signal with a 1 KHz clock produced by the mono-stable oscillator U48a. Each occurence of the 4 msec Tone Decoder output is converted into a 1 msec pulse by U55 which presets counter U59 with a binary 2 (0010) and sets the output of flip-flop U45a to a logic "1". When preset occurs the ripple carry output of U59 changes to logic "0" clearing the output of U45a to a logic "0". The counter continues to state 15, at the 1 KC rate (1 msec), which forces the ripple carry output hi sampling the output of U45a by U61b. Counter U59 remains in state 15 until pushed to state 2 by detection of another address burst. If only one address burst occures during the 14 msec period the output of U61b will be a logic "0". More than one burst in 14 msec forces U45a to a logic "1" and presets the counter to state 2. Since the counter never reached state 15 the ripple carry out remains low and does not clear flip-flop U45a to state "0". Additional pulses spaced less than 14 msec repeat this reset process until a period of at least 14 msec lapses with no pulses. This period allows the counter to reach state 15 where the rising edge of the ripply carry output forces U61b to sample the output of U45a. This time U45a contains a logic "1" indicating more than one pulse has occured in 14 msec defining a no loopback condition.

3.3.5 Fault Locate (Sheet 3)

The Fault Locate circuits are triggered by a valid loopback condition as detected by the Loopback Detector Circuits. Once loopback is detected it is necessary to determine its quality, Good/Bad. The Fault Locate Circuit defines a timed sequence which allows 200 msec for framing, 2 sec for Good/Bad error detection and 2 sec to display the Good/Bad condition.

A counter chain consisting of flip-flop U52a and decade counters U53, 56, 60 divide down the 1 KC oscillator U48a to a 2 sec clock. These counters are normally reset until either a parity error or loopback condition is detected. The 2 sec clock is applied to a two stage shift register U63.

The shift register controls the counter sequence. A valid loopback condition sets the outputs of the shift register both to logic "1". This removes reset from the first two decade counters U53, U56. The third counter U60 is held in reset by the loopback pulse applied through U47b. Decade counter U56 overflows after 200 ms and resets the loopback flip-flp U61b through U61a. This removes the reset on U60 and provides a 200 msec period for receiver re-framing. All three counters continue to count up from reset. When the third counter U60 overflows a period of two seconds has elapsed since the completion of the 200 msec interval. During this time counters in the Error Counter circuitry have been counting parity errors. More than 15 during the 2 sec interval defines a BAD condition. The overflow of U60 transfers a zero to the output of U63a. The outputs of U63a and U62a are decoded by U51a, b and enable the good and bad indicators. Counter chain U53, 56, 60 continue to count until U60 overflows 2 sec later. This transfers a "0" to the output of U63b marking the end of the Good/Bad indicator display period.

The NAND gates U62a, b form an RS flip-flop. Loopback detection sets the output of U62a to a logic "1" defining the fault locate period. This output turns on the loopback indicator, disables the de-scrambler and inverts the received data. The RS flip-flop is reset at the end of the second 2 sec interval when the output of U63a becomes a logic "0".

The Fault Locate Circuit also determines the two second error count interval to determine the 10^{-6} error indication. Detected parity errors reset the second stage of the shift register U63b. This removes the reset of the counter chain U53, 56, 60. Counter U60 overflows after 2 sec transfering a "0" to the output of U63b ending the 2 sec interval. Counters in the Error Counter circuit are enabled during this time and determine the 10^{-6} threshold of 31 errors in 2 sec. Note that none of the fault locate function has been activated.

3.3.6 Error Counter (Sheet 4)

The error counters are enabled for 2 sec intervals as defined by outputs of the Fault Locate Circuitry. Parity errors are counted by counter U50 and flip-flops U49a, b. These components are normally reset. The reset is removed during the 2 sec interval as controlled by U51b.

Counter (U50) overflows after 15 errors setting the output of U49b to a logic "1". After the next 15 errors, total 31, the output of U49a becomes a logic "1". Detection of the first 15 errors sets the Good/Bad indicator flip-flop U57a Hi if loopback (Fault Locate) has been detected. Detection of 31 errors (second block of 15) triggers the 2.5 sec one shot circuit U54a turning on the 10^{-6} error indicator for 2.5 sec. The 31 error detector also sets the 10^{-6} error history flip-flop U57b turning on its associated indicator.

Each error detected stimulates a 250 msec one shot U54b which turns on the single error indicator. Single errors also set the Single Error History flip-flop U52b turning on its associated indicator.

The history flip-flops U52b and U57b are reset by the front panel History Reset Switch. Note also that all error indicators are forced off during the receiver fault locate mode.

3.3.7 De-scrambler (Sheet 2)

The De-scrambler removes the effects produced by the data scrambler in the transmitter section.

The De-scrambler consists of a seven stage shift register (U20, 11b). Received data is sampled by D-type flip-flop U11a entering the shift register at U20. The fourth and seventh stages of the shift register are exclusive-ORed by U12b and passed through a disable gate U9c. This output is exclusive-ORed with the received data from U11a by U12c whose output represents de-scrambled data.

During fault locate testing the transmitter disables its scrambler and the addressed repeater inverts the data stream when it loopbacks. Likewise, the receiver disables its de-scrambler at U9c and inverts the de-scrambler output at U12a whenever the fault locate mode is detected.

3.3.8 Frame Synchronization

Data received by the Test Set consists of data bits mixed with frame bits. The frame bits represent a code which the receiver uses to separate the received signal into its various components consisting of frames, sub-frames, frame bits, marker bits, control bits, and data bits. The receiver contains a frame bit generator similar to that in the transmitter. Frame synchronization is obtained when the bits generated by the receiver's frame bit generator match bit by bit with those in the received signal.

Frame code bits are spaced every 85th received signal time slot. A divide by 85 counter consisting of U15, 18, 14b determine these positions. Flip-flop U8 inhibits the divide by 85 counter for one clock period whenever it receives an F-ADJ. signal from the F-BIT synchronization circuit.

F-BITS are generated by counter ($\div$ 8) U23 and decoder logic U21b, U21c, and U19b. This produces a 001100...11 pattern which is re-clocked by U17a and compared with the received signal at exclusive-OR gate U19c. The output of U19c is sliced in the center of the time slot by U16a. The slicing signal used by U16a is generated by U17b which samples the output of the F-BIT counter U23, at each F-BIT time slot. The output of U16a is low whenever the F-BIT generator and received signal are identical. This output is used by the F-BIT synchronization circuit.

M-BITS (Fig. 5-7 Sheet 3) are generated by counter U37 ($\div$ 7) and decode logic U24a and U32c. Flip-flop U31 inhibits this counter one clock cycle whenever it receives a signal from the M-BIT synchronization

circuit. The output of U32c is re-clocked by U33a and U33b. The output of U33b coincides with the center of an M-BIT time slot (M5, 6, 7) and is used by U38a to sample the output of exclusive-OR gate U24a. M-BITS are compared with the data signal at U24a. The output of U38a is passed to the M-BIT synchronization circuit and is a logic "0" if the M-BIT generator equals the received signal.

F-BIT synchronization is determined by U29, U30 and U36. A divide by 15 counter U29 separates the F-BITS into blocks of 15. To acquire synchronization this counter must reach state 15 which clocks flip-flop U36a. An error from the F-BIT compare circuit at this time will reset the counter. Therefore, 15 consecutive error free F-BITS must be found to acquire F-BIT synchronization. Once synchronization is found, U29 cannot be reset by F-BIT errors as the output of U28b has been switched off by flip-flop U36a. Counter U30 divides by three, and is reset each time counter U29 reaches 15. If U30 counts 3 F-BIT errors before it is reset, it will reset flip-flop U36a declaring an out of synchronization condition.

M-BIT synchronization is determined by U43, U44, U45b, U36b. Counter U43 divides by three and increments once each frame. To acquire synchronization three consecutive frames ("010" patterns) must pass without error. Counter U43 is reset whenever an M-BIT compare is in error. At count 3 U36b is clocked setting its output to "0". This inturn inhibits the reset of U43 by compare errors at gate U41a. Once in synchronization a shift register consisting of U44b and U45b monitor the M-compare circuit for errors. This register is reset each time U43 reaches a count of 3. Therefore, if more than 2 errors occur in 3 consecutive frames the output of U45b becomes a logic "0". This resets U36 and declares the circuit out of M-synchronization.

Both M-BIT and F-BIT synchronization must be achieved to extinguish the front panel frame loss indicator as controlled by gate U35c.

As a precaution against false framing, the M-BIT circuits are given 15 frames to acquire synchronization. This is determined by counter U64, clocked by the F-BIT divider U36a. If M-BIT synchronization is not obtained by this time, a signal from U64, when it overflows, is combined with an output from U29 at gate U35b to push the F-BIT circuit out of sync. The correction is introduced at U28c producing an F-ADJ. pulse.

Both circuits achieve synchronization by inhibiting their respective counters U23 and 37 for one clock cycle. These signals are designated F-ADJ (adjust) and M-ADJ. The F-BIT adjust causes an apparent slippage by one 44.736 MHz data cycle between the F-BIT generator and the received signal. The M-BIT adjust produces an apparent slippage of one frame code bit between the M-BIT genrator and the received data. These slippages eventually align the M-BITS and F-BITS generated in the receiver with those in the received signal, which defines synchronization.

3.3.9 Rear Panel Connectors (Sheet 1)
Three rear panel BNC connectors provide access to the Received Data, Received Clock and detected Parity Errors. These output ports are short circuit protected and drive coaxial cable terminated in 75 ohms. The signal levels are 0 to +2V $\pm$ 10%. Each connector is interfaced to the rest of the receiver circuits with a drive transistor (Q2, Q3 or Q4) and an ECL to TTL level translator (U3a, b or d).

3.3.10 Parity Generator (Sheet 2)
The Parity Generator performs a real time bit by bit modulus 2 addition of all data bits in the composite received data - frame signal. The result of this addition over one frame determines the parity of the data contained in that frame. Even parity, addition results in logic 0, indicates an even number of 1's in the data. Odd parity indicates an odd number of 1's and results in a logic 1 addition.

A Gap Clock is generated by flip-flop U13a and b and NOR-gate U10a. The Gap Clock has spaces (gaps) every 85 cycles synchronized to the frame bit positions. This clock can therefore be used to identify data bits and ignore frame bits in the composit received signal.

The modulus 2 addition is executed by exclusive-OR gate U19a. This gate adds a new data bit to the sum of all previous data bits. The sum is stored by flip-flop U22a which is clocked by the Gap Clock.

The sum of data bits over one frame is stored by flip-flop U22b which is clocked by the frame bit M-1. Bit M-1 marks the boundary between the end of one frame and the beginning of another. The output of U22b provides a history of what the sum of all data bits was just before a new frame starts. The output of U22a contains the present bit by bit sum of all data bits. Adding these two quantities together at U24b and storing the result at the end of the frame (U25a clocked by M1) results in the parity calculation of data over the new frame only. This result is used by the parity error detector.

3.3.11 Parity Errors (Sheet 3)
The parity error circuit compares the parity of all data bits over the previous frame with the parity frame bits (M3, M4) of the present frame. The parity generator calculates parity of all data bits over a frame.

Flip-flops U39a + b form a shift register which is clocked synchronously with the position of frame bits M3 and M4 in the received data signal. This clock is generated by flip-flops U34a + b. At the end of any frame period U39a and U39b will contain the value of parity bit M4 and M3, respectively. These bits are ORed together by U10b and compared with the output of the parity generator (Sheet 2) by exclusive-OR gate U24c. If these two inputs are identical, no error is detected. The presence or absence of an error is stored by U38b which is clocked at the end of a frame by M1. The output of U38b is gated with the M1 frame bit at U10c. This insures that consecutive frames in error are not treated as only one error.

3.4 Display Board (Fig 5-1)

The Display Board provides a mechanical apparatus for mounting all front panel indicators and switches. In addition, electronics are present which provide switch de-bounce, indicator drive and an interface for the high speed data exchange between the test set and equipment under test.

Indicator drive power is derived from open collector TTL NAND gates and inverters, (U3, 4, 5). A simple buffer operation is provided by U5 to connect the LOOPBACK, GOOD, BAD and WAIT indicators to control signals residing on the transmitter and receiver boards. The FRAME LOSS and ERROR indicators are forced on during a signal loss condition through U5f, U4b, U4c, U4d and U4f. The FRAME LOSS, 10^{-6} ERROR and SINGLE ERROR Indicators are inhibited by NAND gate U3 during the wait period plus approximately three seconds. This eight second delay is produced by the monostable flip-flop U7. Transistors Q4 and Q5 provide an interface between C-MOS located on the Receiver Board and the TTL indicator drivers.

The Single Error, 10^{-6} Error, Test and Stress Test Switches are each de-bounced by NAND gates U1 and U2 connected as RS flip-flops. The History Reset Switch is de-bounced by an RC filter consisting of R11, R12 and C1. Outputs of the Test and Stress Test flip-flops are combined by NAND gate U8a and trigger the eight second monostable flip-flop U7. Transistor Q3 provides a C-MOS to TTL interface.

Data from the transmitter board is connected to Line Receiver U6b which drives transistors Q1 and Q2. This circuit interfaces the 110 ohm line impedance from the transmitter board to a 75 ohm front panel connector, DATA OUT. The output signal is ECL compatible and short circuit protected.

Data from the equipment under test passes through a 75 ohm front panel connector, DATA IN, to the display board line receiver U6a. Resistors R21 and R22 present a 75 ohm terminating impedance connected to -2.0 volts. The line receiver drives the 110 ohm cable to the receiver board.

3.5 Power Supply (Fig. 5-9)

The Power Supply provides +5.0 and -5.2 V $\pm$ 5% to all test set electronics. Voltage regulation is controlled by two hybrid circuits U1 and U2. Circuit U1 provides the +5.0 volt supply in conjunction with rectifier diodes CR3, CR4 and filter capacitors C1, C3, C5. The -5.2 volt circuit is an adjustable type controlled by voltage divider resistors R1 and R2. Diodes CR1 and CR2 plus capacitors C2, C4, and C6 complete the supply. All components are mounted on a printed wire board, heat sink configuration. Transformer T1 is chassis mounted.

4.0 CALIBRATION

4.0.1 General

To perform Test Set calibration it will be necessary to remove the outer case.

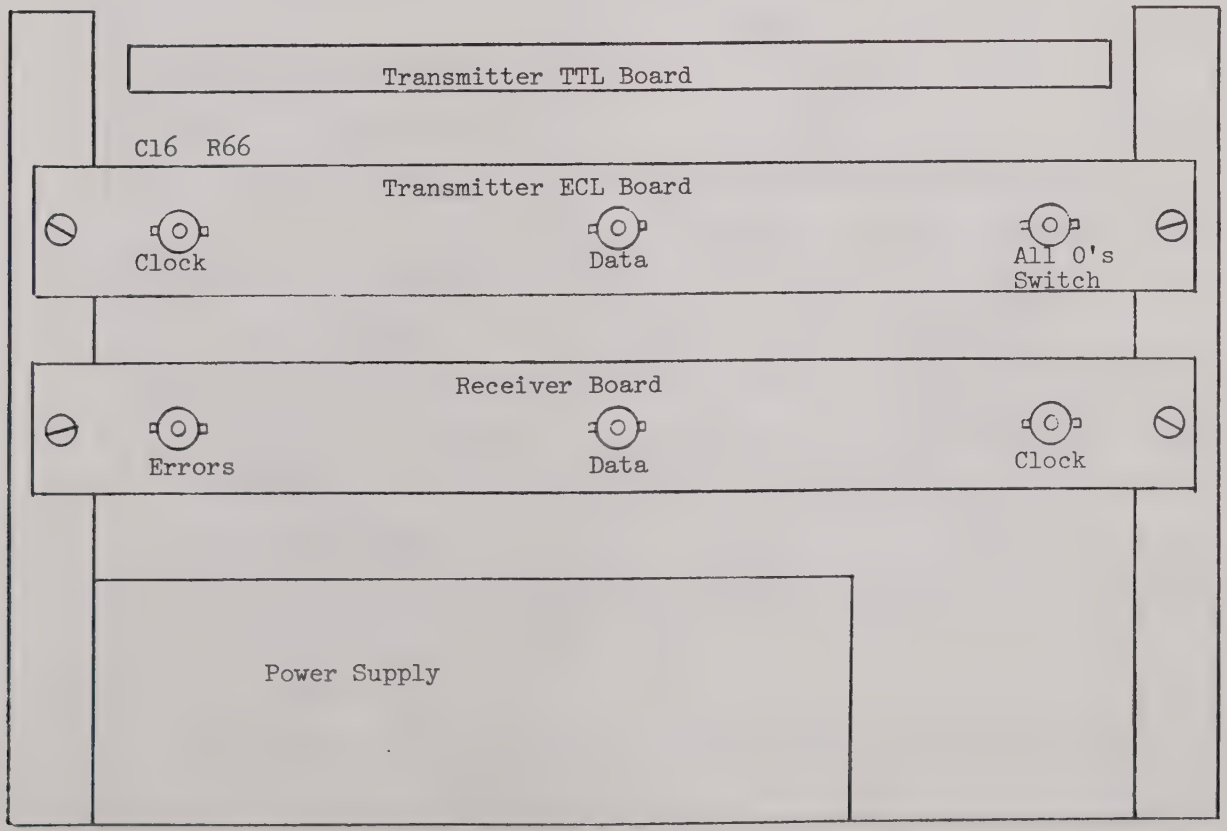
CAUTION: Be sure power cable is disconnected from Test Set before proceeding.

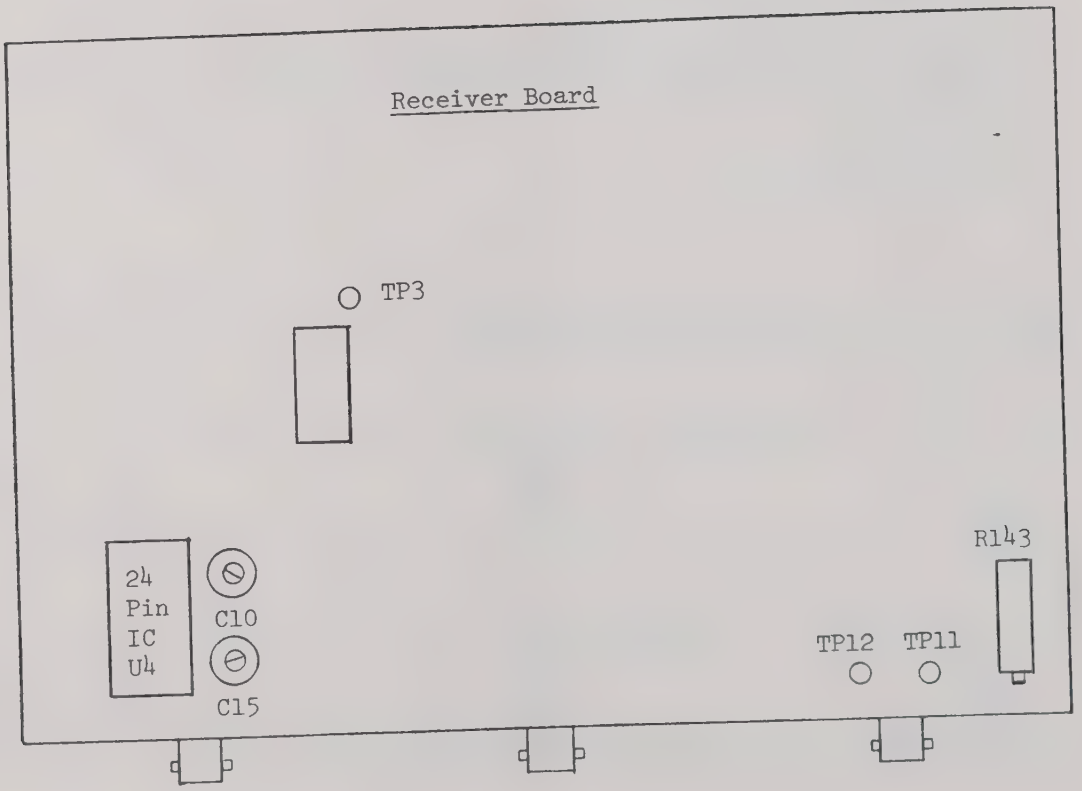
The outer case is held to the inner chassis by ten, number six, Philips head screws located on the rear panel. Remove all screws completely and pull unit from case using the two front panel handles.

It will be necessary to apply AC power to the unit in order to perform calibration. The unit should be connected to a three prong AC outlet to insure proper chassis to earth grounding. A shock hazard exists in the immediate area surrounding the transformer, fan and front panel fuse, line cord connector.

Connect the Test Set to the 60 Hz, 110V line via the line cord provided. Turn the power switch on, which should light its internal lamp. The Test Set should be powered for approximately 30 minutes before calibrating.

4.0.2 System Architecture



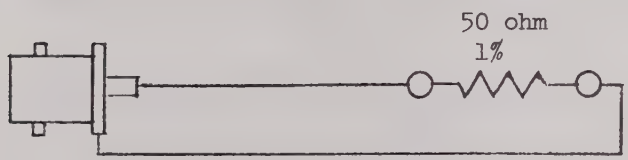

Receiver Board
TP3
24
Pin
IC
U4
C10
C15
R143
TP12
TP11

4.1 Test Equipment

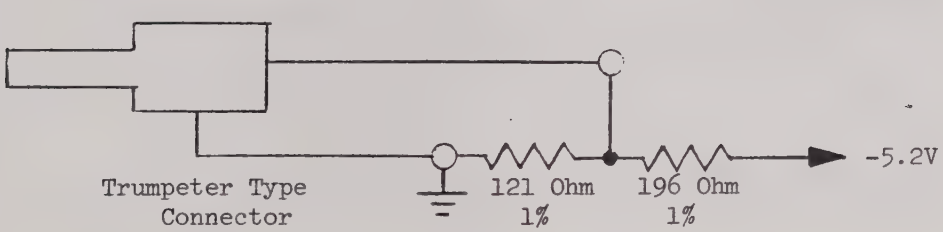
1. Frequency Counter - 7 digit display, 50 MHz minimum.

2. Oscilloscope - Textronics 7000 series or equiv.

3. 50 Ohm Load



4. 75 Ohm Load



4.2 Transmitter Calibration

4.2.1 Crystal Oscillator 44.736 MHz

1. Connect the 50 ohm load to the transmitter clock BNC connector

2. Connect the frequency counter across the 50 ohm load and set its controls to measure frequency.

3. Adjust capacitor C16 for a reading of 44.736 MHz $\pm$ 100 Hz.

4. Remove the counter and connect the oscilloscope across the 50 ohm load.

5. Adjust R66 to achieve a clock signal having approximately 50% duty cycle.

4.3 Receiver Calibration

Remove the two screws that hold the receiver board to the frame located on either side of the BNC connector bracket. Pull the card a few inches out without disconnecting any cables.

4.3.1 Phase Lock Loop

1. Loop back the Test Set by connecting a cable between the DATA IN and DATA OUT front panel ports.

2. Locate the 24 pin IC, U4. Adjust the oscilloscope to measure a DC voltage of 700 mv (Vert Amp. 500 mv/Div.).

3. Place scope probe on Pin 9 and adjust C15 for a reading of 700 mv ± 50 mv.

4. Push and hold All 0's Switch. Note that front panel indicators; LOSS SIGNAL, LOSS FRAME and SINGLE ERRORS are off.

4.3.2 Tone Decoder

1. Connect the oscilloscope to TP3. Vertical Amp. to 2V/Div and horizontal time base to 5 millisecond.

2. Set the Site Address thumbwheel switches to 99. A square wave having a period of approximately 8 milliseconds should appear on oscilloscope each time the Test Switch is pushed when the Wait Indicator is out.

3. Adjust capacitor C10 for a 50% duty cycle signal.

4.3.3 Oscillator 1 kc

1. Connect the frequency counter to TP11.

2. Adjust R143 for a reading of 1 KHz ± 10 Hz.

4.4 Operational Checks

Perform the Self Test procedure in Section 2.1.

Diagrams

Fig. 5-1: FT3 Test Set Display Board Schematic (DFT3-100/0)
Fig. 5-2: FT3 Display Board P.C. Assembly (CFT3-200/B)

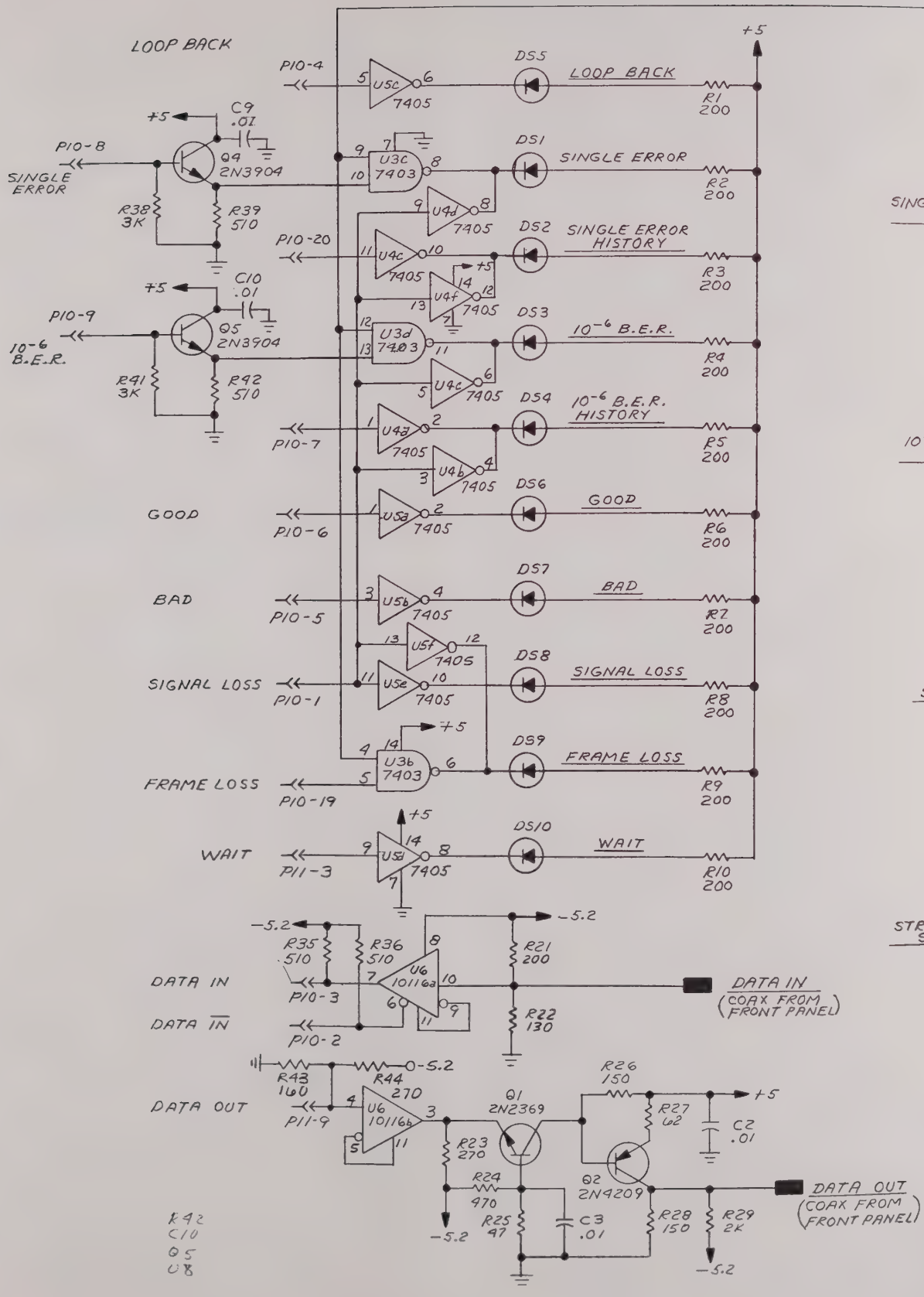
Fig. 5-3: FT3 Test Set Transmitter (ECL) Schematic (DFT3-101/E, 2 Sheets)
Fig. 5-4: FT3 Transmitter (ECL) P.C. Board Assembly (DFT3-201/D)

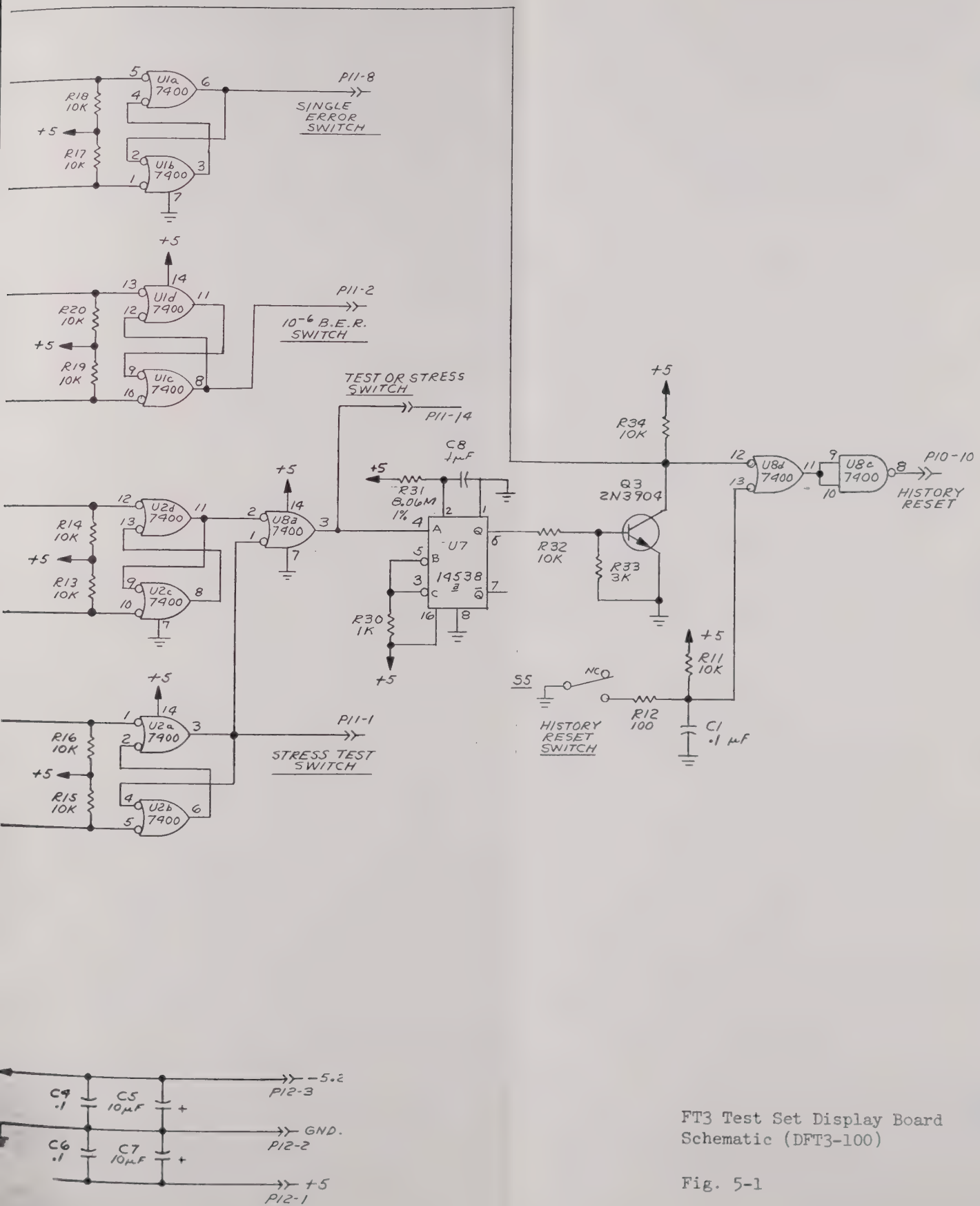
Fig. 5-5: FT3 Test Set Transmitter (TTL) Schematic (DFT3-102/B, 2 Sheets)
Fig. 5-6: FT3 Transmitter (TTL) Board Assembly (CFT3-202/D)

Fig. 5-7: FT3 Test Set Receiver Schematic (DFT3-103/C, 4 Sheets)
Fig. 5-8: FT3 Receiver P.C. Board Assembly (DFT3-203/D)

Fig. 5-9: FT3 Test Set Power Supply Schematic (CFT3-104/A)
Fig. 5-10: FT3 Power Supply Assembly (CFT3-207/A)

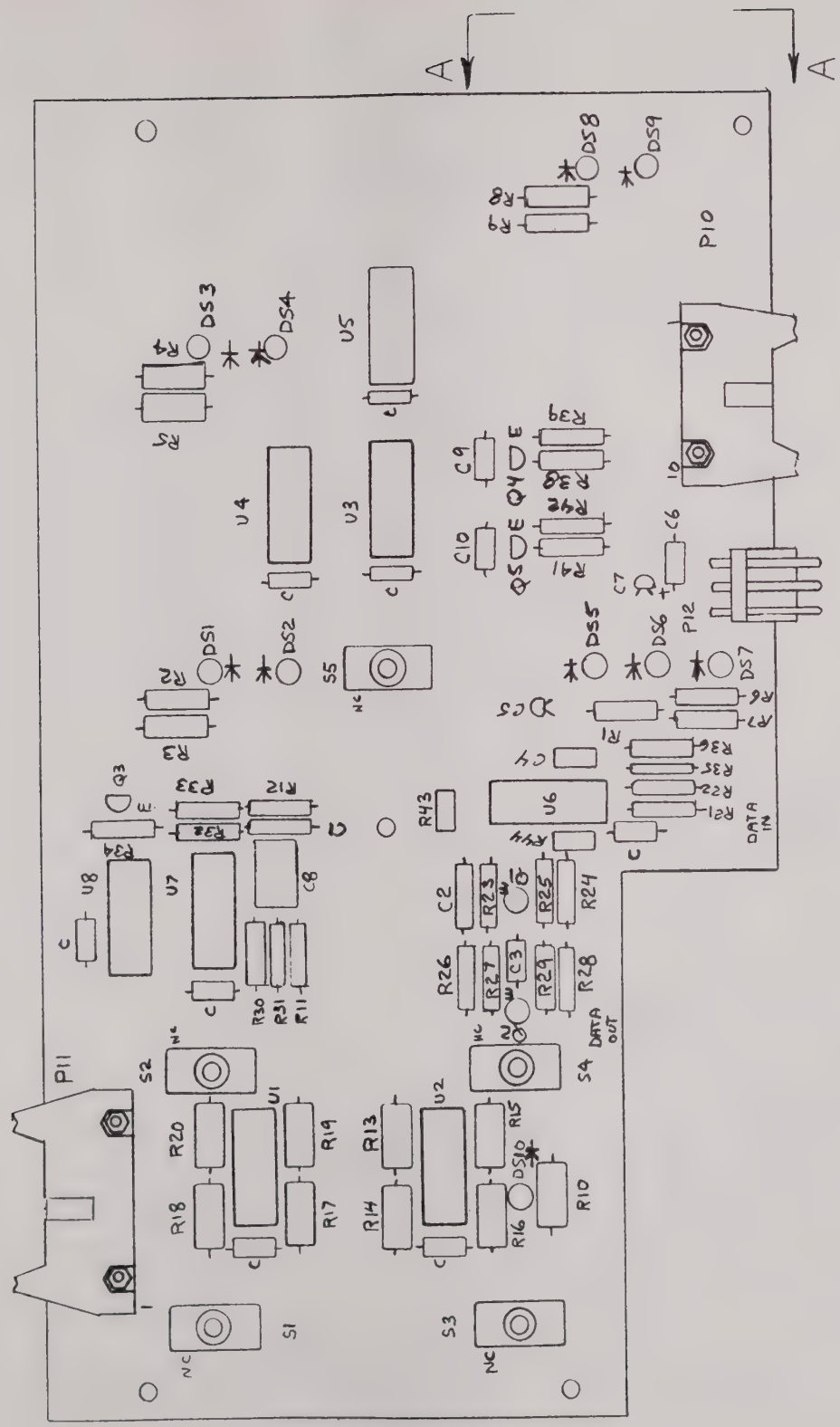
Fig. 5-11: FT3 Test Set Interconnection Schematic (DFT3-105/A)


LOOP BACK
P10-4
U5c 7405
DS5
LOOP BACK
R1 200
+5
C9 .01
P10-8
SINGLE ERROR
Q4 2N3904
R38 3K
R39 510
U3c 7403
U4d 7405
DS1
SINGLE ERROR
R2 200
P10-20
U4c 7405
U4f 7405
DS2
SINGLE ERROR HISTORY
R3 200
C10 .01
P10-9
10⁻⁶ B.E.R.
Q5 2N3904
R41 3K
R92 510
U3d 7403
U4c 7405
DS3
10⁻⁶ B.E.R.
R4 200
P10-7
U4a 7405
U4b 7405
DS4
10⁻⁶ B.E.R. HISTORY
R5 200
GOOD
P10-6
U5a 7405
DS6
GOOD
R6 200
BAD
P10-5
U5b 7405
DS7
BAD
R7 200
SIGNAL LOSS
P10-1
U5f 7405
U5e 7405
DS8
SIGNAL LOSS
R8 200
U3b 7403
DS9
FRAME LOSS
R9 200
FRAME LOSS
P10-19
WAIT
P11-3
U5d 7405
DS10
WAIT
R10 200
-5.2
R35 510
R36 510
U6 10116a
R21 200
DATA IN
P10-3
DATA IN
P10-2
R22 130
DATA IN (COAX FROM FRONT PANEL)
R43 160
R44 270
DATA OUT
P11-9
U6 10116b
Q1 2N2369
R26 150
R27 62
C2 .01
R23 270
R24 470
R25 47
C3 .01
Q2 2N4209
R28 150
R29 2k
DATA OUT (COAX FROM FRONT PANEL)
S1
SINGLE ERROR SWITCH
S2
10⁻⁶ B.E.R. SWITCH
S4
TEST SWITCH
S3
STRESS TEST SWITCH
NC



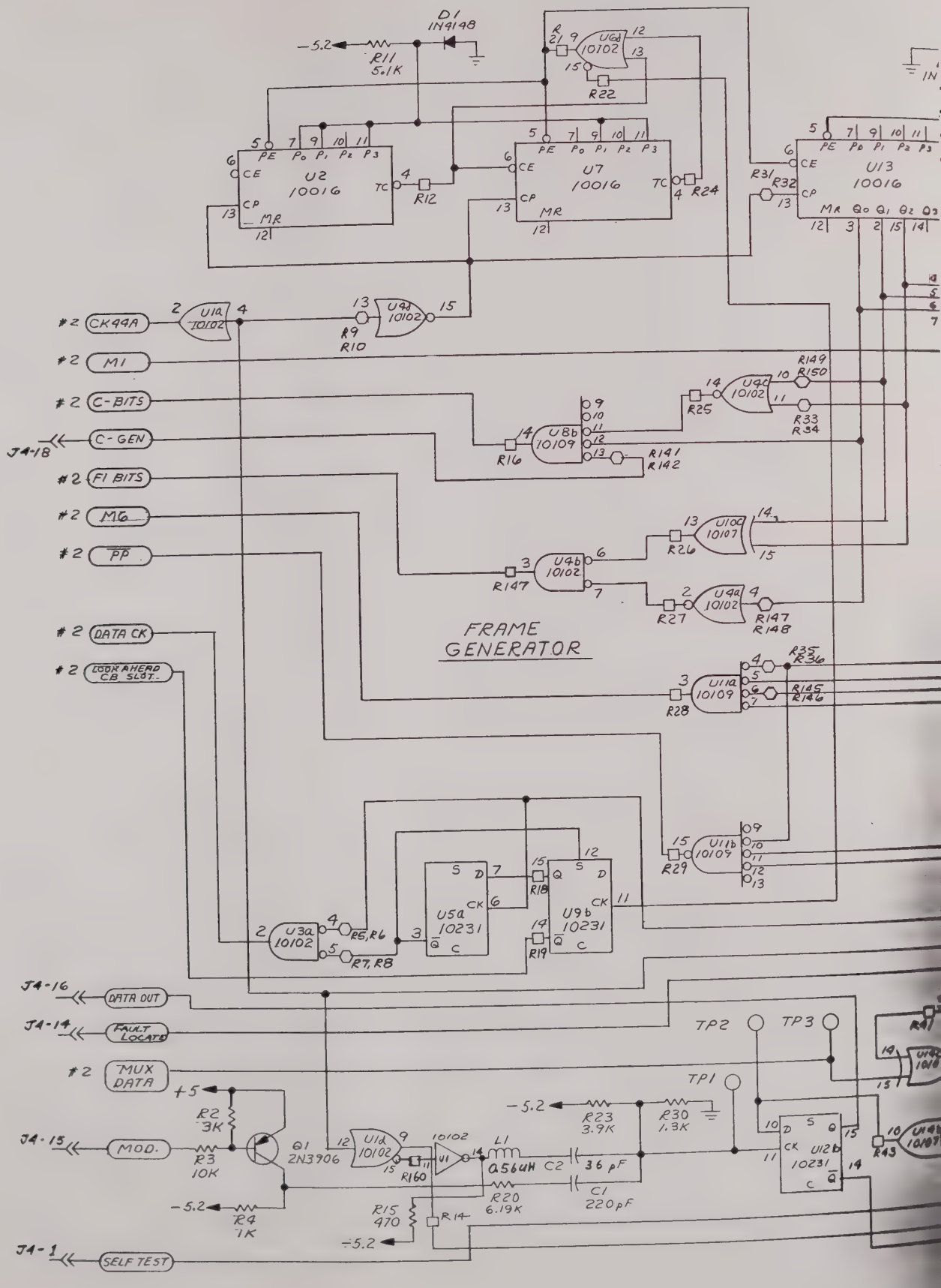
FT3 Test Set Display Board Schematic (DFT3-100)

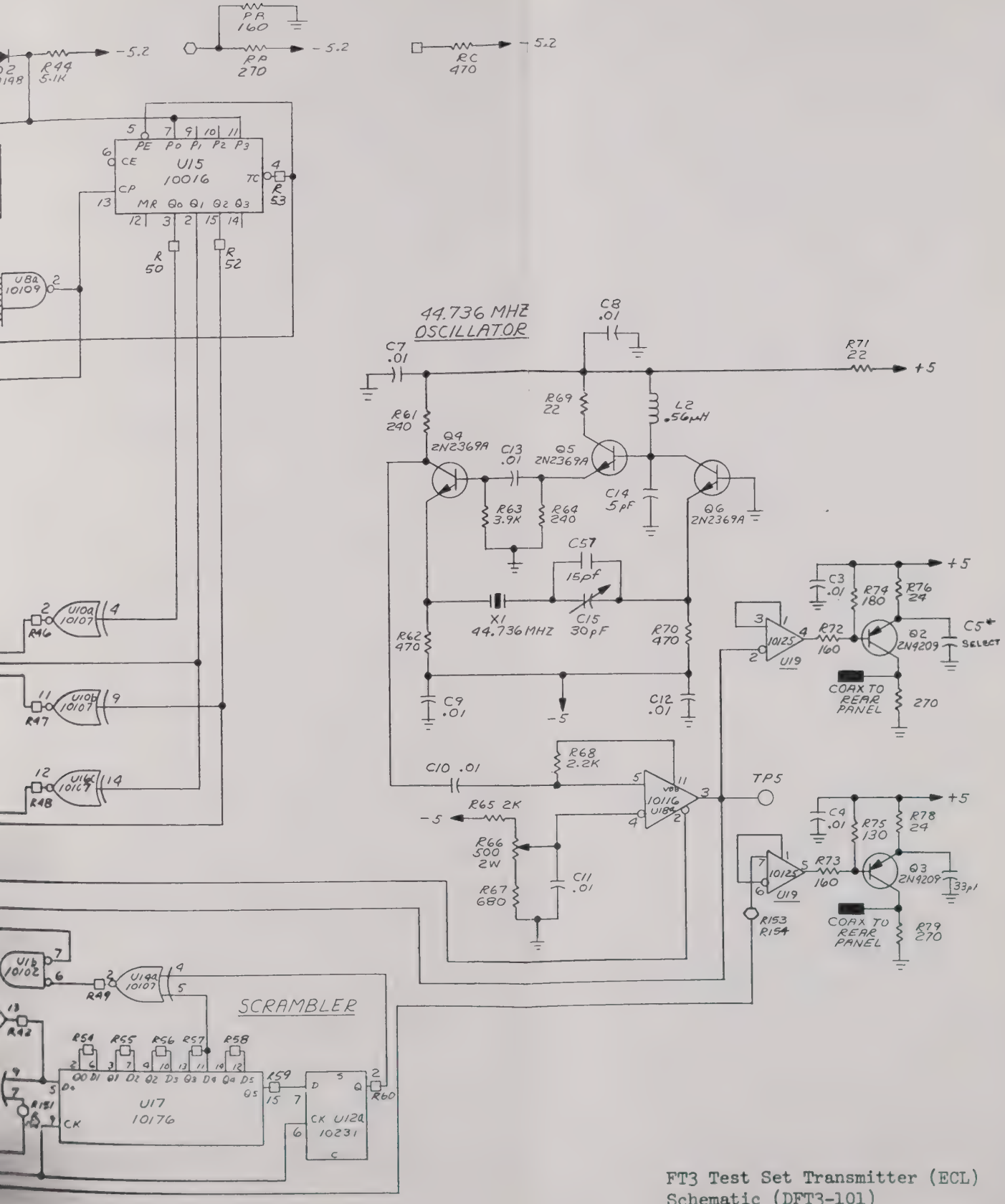
Fig. 5-1



FT3 Display Board P.C. Assembly
(CFT3-200)

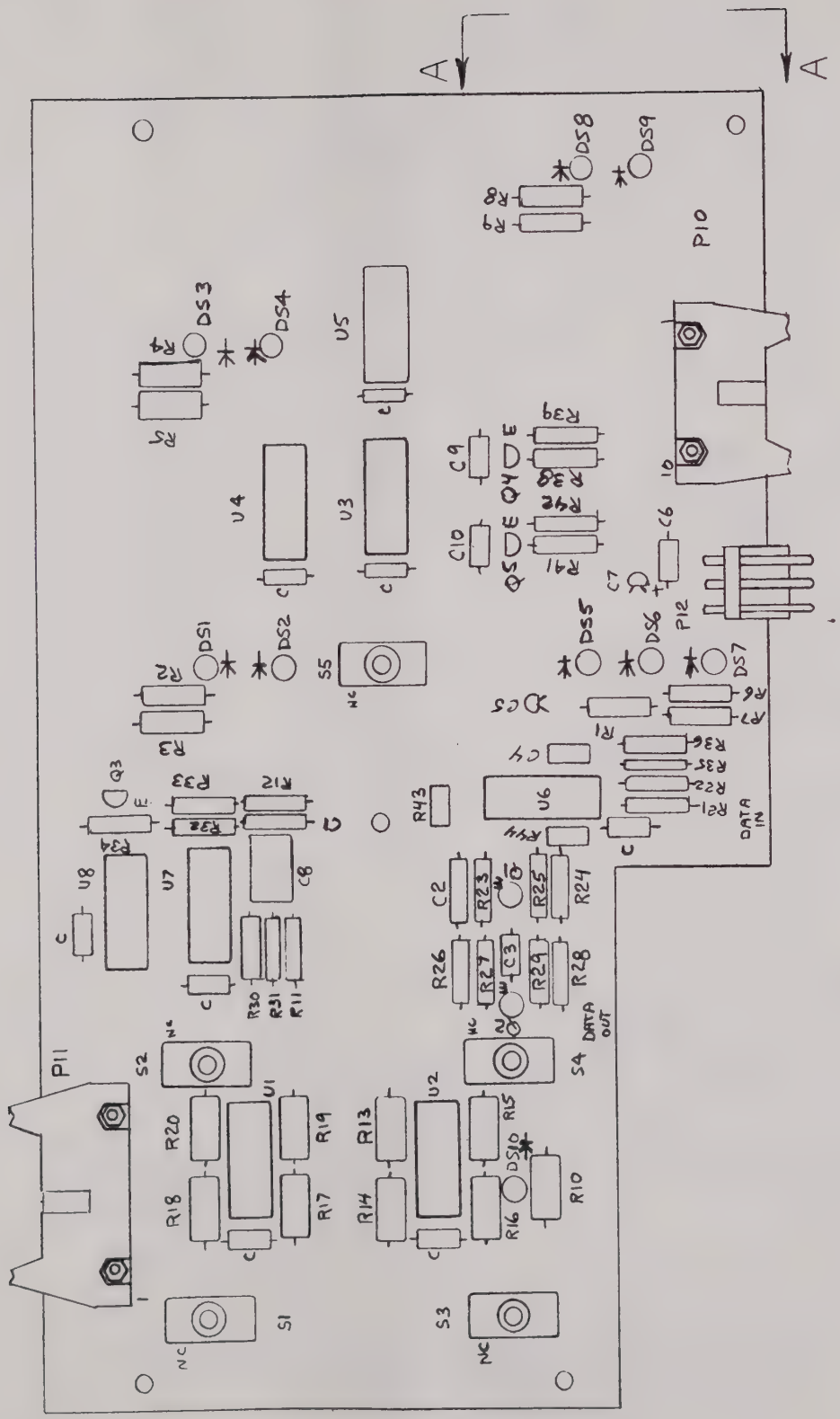
Fig. 5-2


FRAME GENERATOR
D1 1N4148
-5.2
R11 5.1K
U6d 10102
R22
U2 10016
U7 10016
U13 10016
R12
R24
R31
R32
#2 CK44A
#2 M1
#2 C-BITS
J4-18 C-GEN
#2 FI BITS
#2 M6
#2 PP
U1a 10102
U9d 10102
R9
R10
U8b 10109
R16
U9c 10102
R25
R33
R34
R149
R150
R141
R142
U10d 10107
R26
U4b 10102
R147
U4a 10102
R27
R147
R148
#2 DATA CK
#2 LOOK AHEAD CB SLOT
U11a 10109
R28
R35
R36
R145
R146
U11b 10109
R29
U5a 10231
U9b 10231
R18
R19
U3a 10102
R6, R6
R7, R8
J4-16 DATA OUT
J4-14 FAULT LOCATE
#2 MUX DATA
TP1
TP2
TP3
+5
R2 3K
J4-15 MOD.
R3 10K
Q1 2N3906
U1d 10102
U1
R160
L1
0.56uH
C2
36 pF
C1
220pF
R20 6.19K
R15 470
R14
-5.2
R4 1K
R23 3.9K
R30 1.3K
U12b 10231
R43
J4-1 SELF TEST



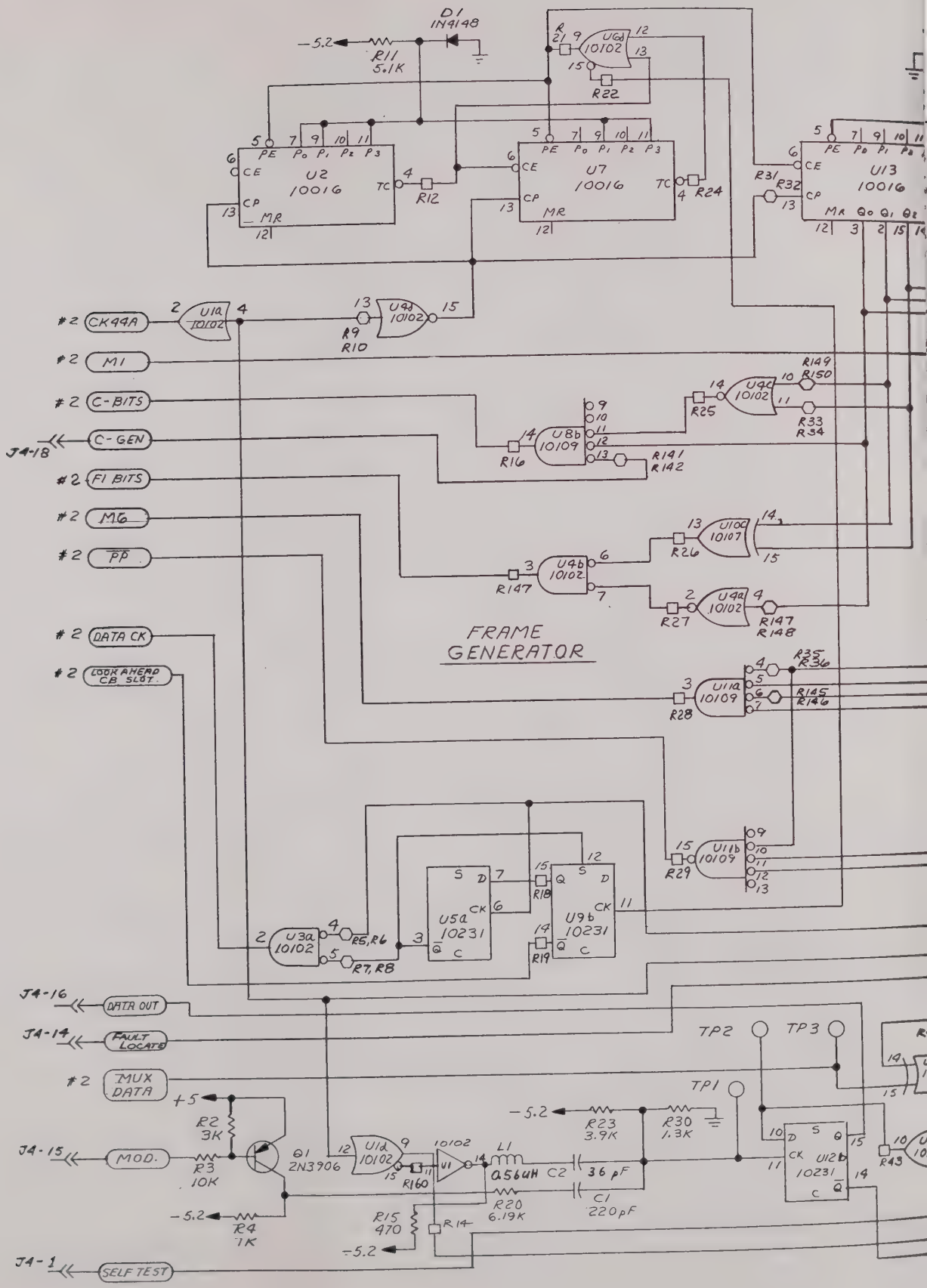
FT3 Test Set Transmitter (ECL) Schematic (DFT3-101)

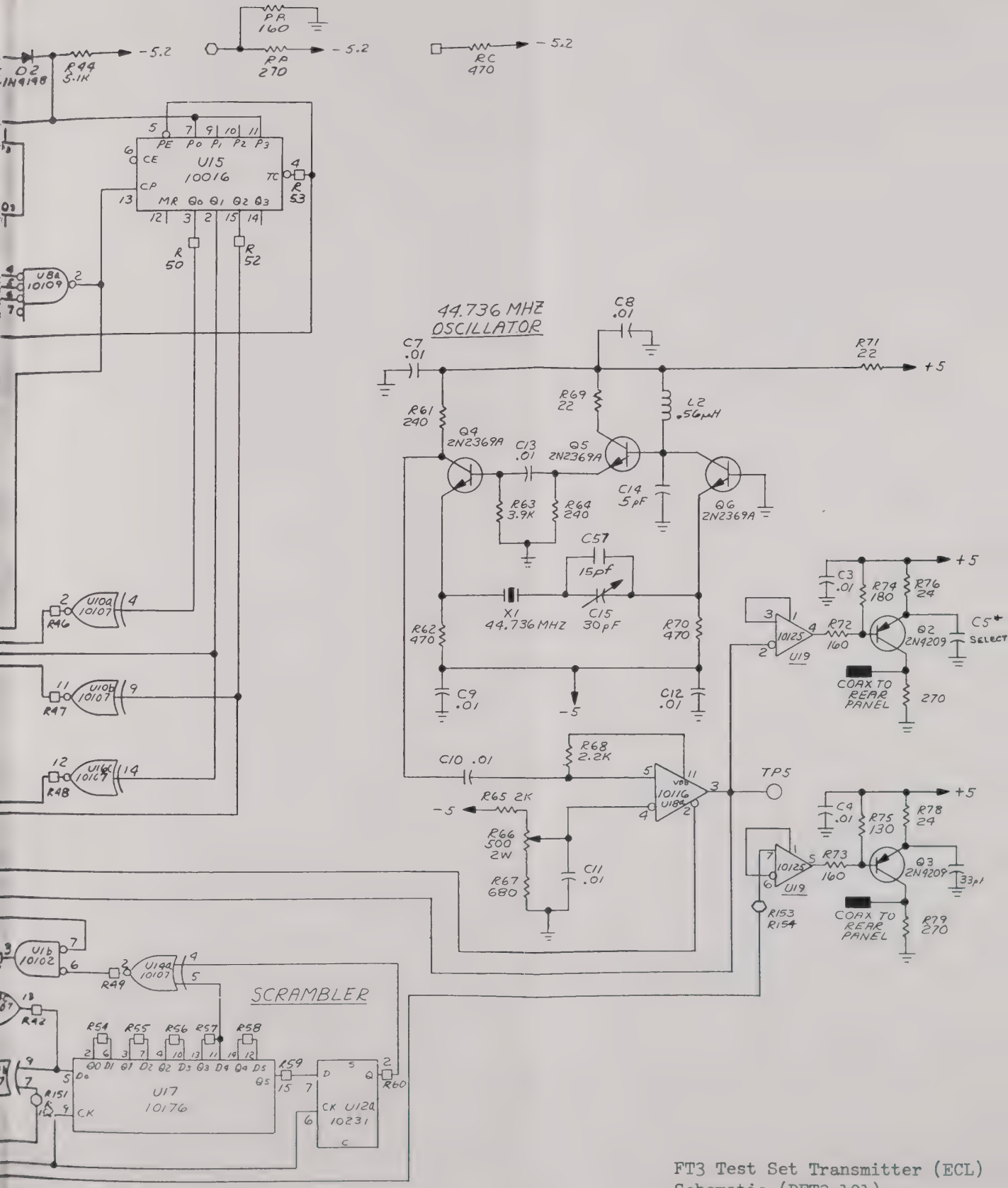
Fig. 5-3 Sheet 1



FT3 Display Board P.C. Assembly
(CFT3-200)

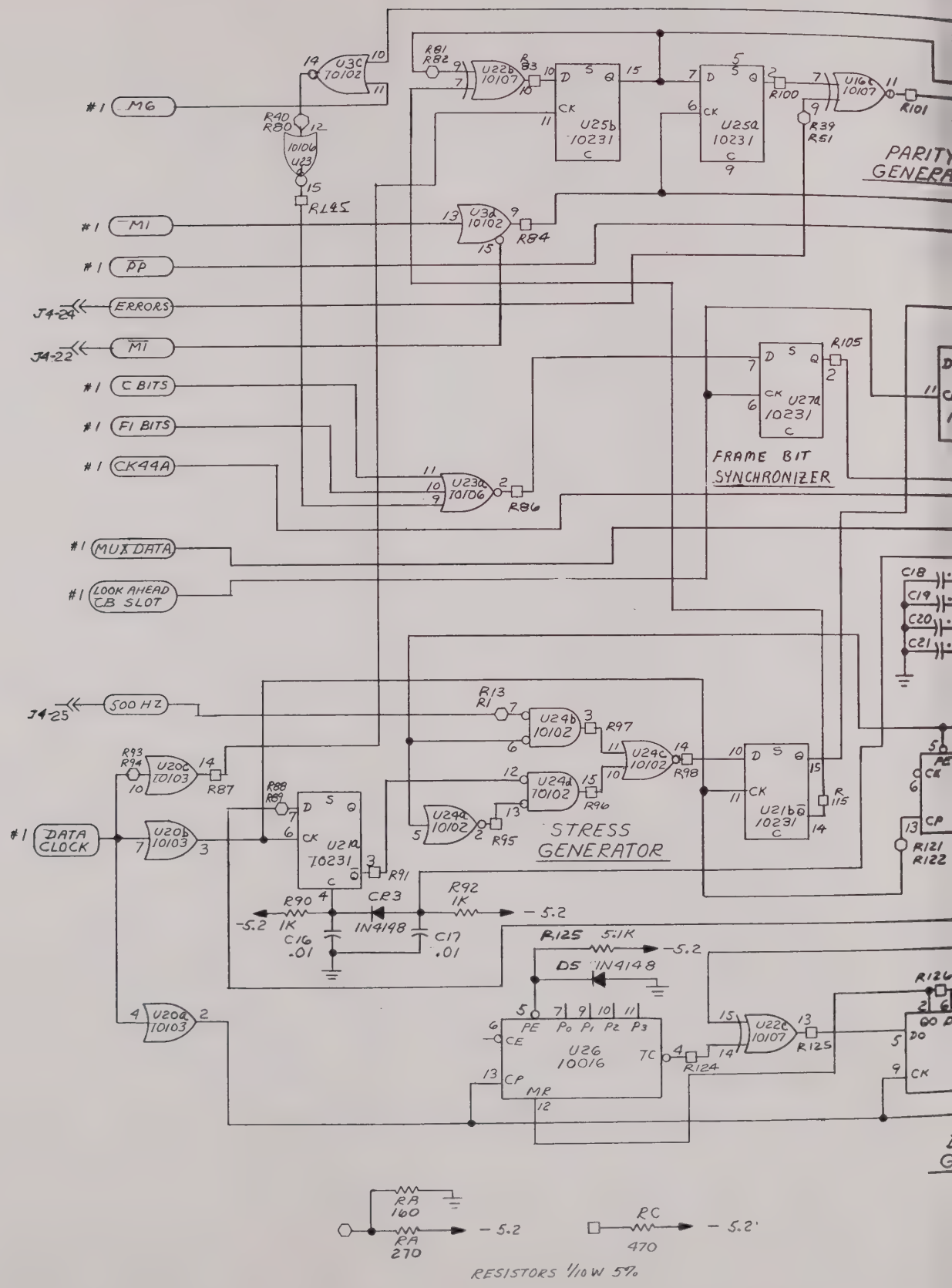
Fig. 5-2

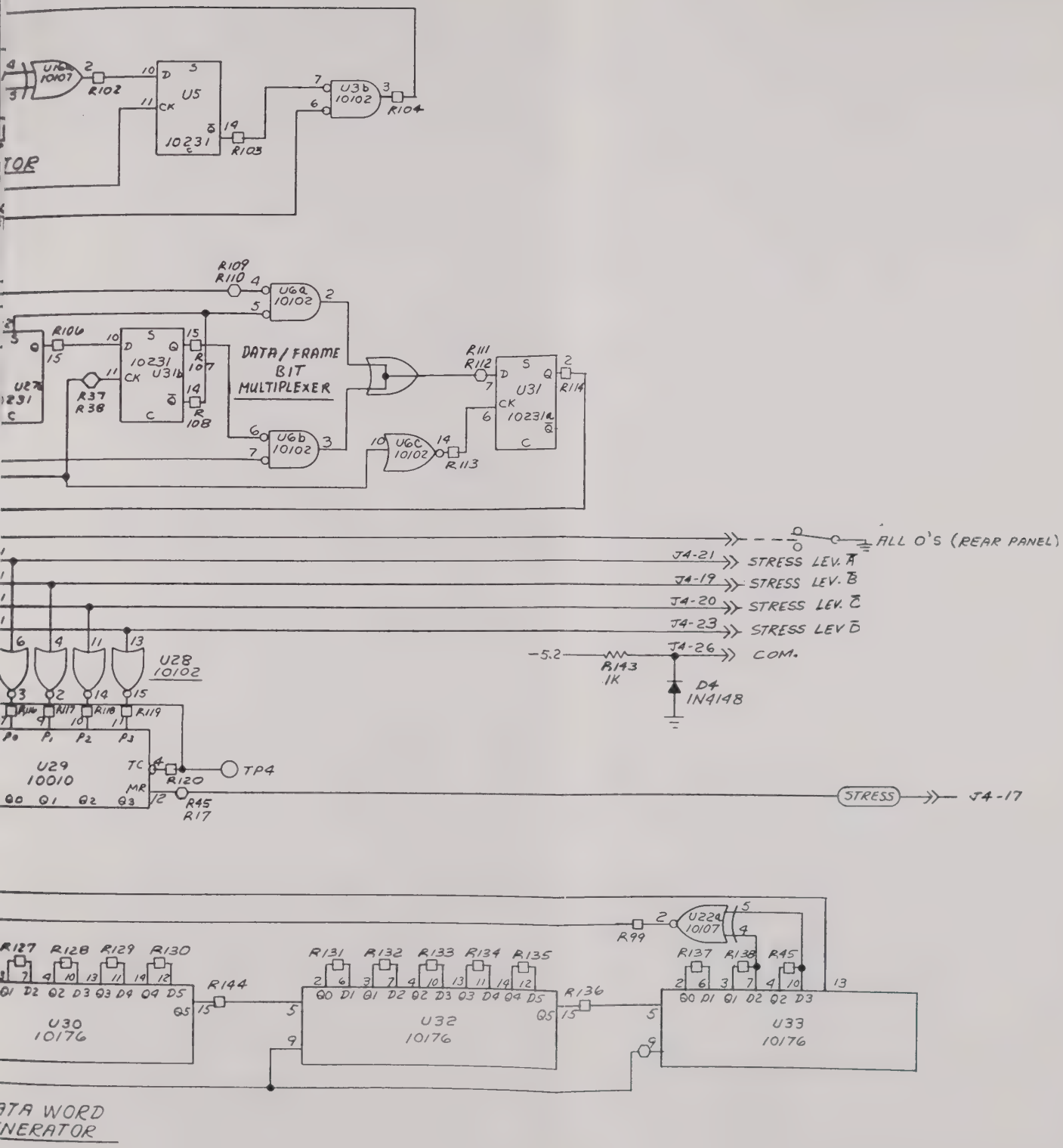

D1 1N9148
-5.2
R11 5.1K
U2 10016
U7 10016
U13 10016
R22
R24
R12
R31 R32
#2 CK44A
#2 M1
#2 C-BITS
J4-18 C-GEN
#2 F1 BITS
#2 M6
#2 PP
#2 DATA CK
#2 LOOK AHEAD CB SLOT
FRAME GENERATOR
R9 R10
R16
R25
R26
R27
R147
R28
R29
R149 R150
R33 R34
R141 R142
R35 R36
R145 R146
R147 R148
R5, R6
R7, R8
R18
R19
J4-16 DATA OUT
J4-14 FAULT LOCATE
#2 MUX DATA
J4-15 MOD.
J4-1 SELF TEST
+5
R2 3K
R3 10K
Q1 2N3906
R4 1K
R160
L1
0.564H
C2 36 pF
C1 220pF
R20 6.19K
R15 470
R14
R23 3.9K
R30 1.3K
TP1
TP2
TP3
R43



FT3 Test Set Transmitter (ECL)
Schematic (DFT3-101)

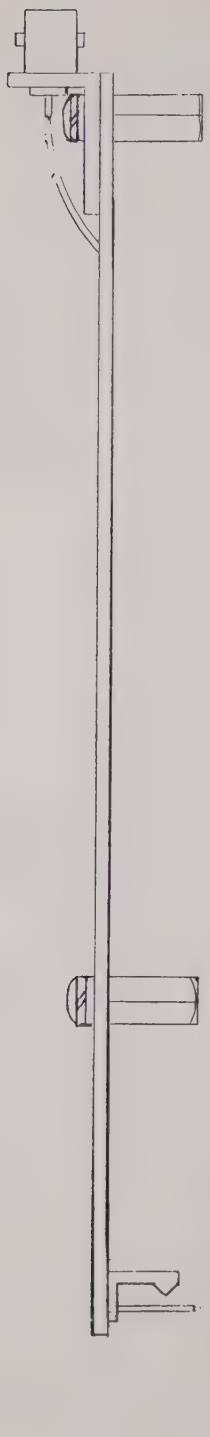
Fig. 5-3 Sheet 1

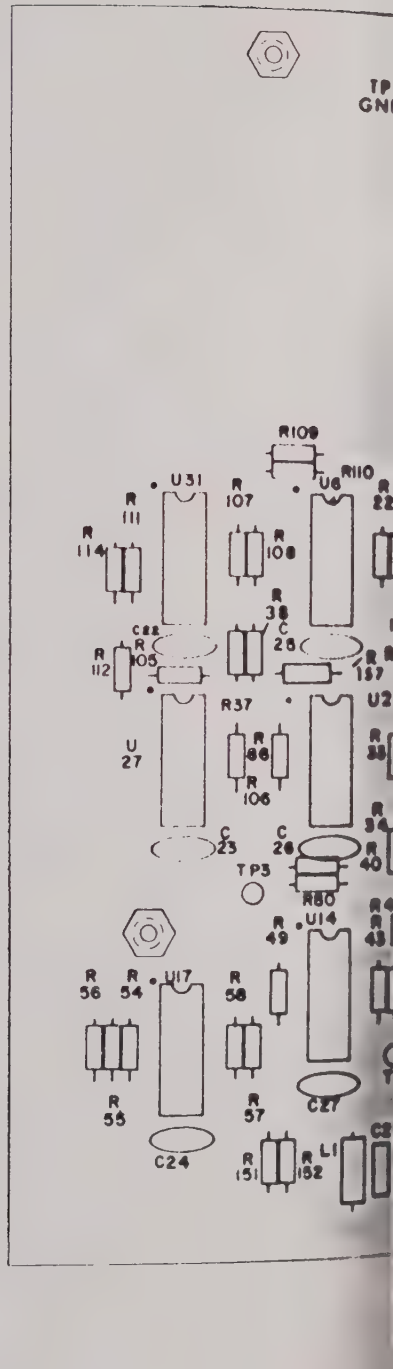

#1 M6
#1 M1
#1 P P
J4-24 ERRORS
J4-22 M1
#1 C BITS
#1 F1 BITS
#1 CK44A
#1 MUX DATA
#1 LOOK AHEAD C.B SLOT
J4-25 500 HZ
#1 DATA CLOCK
PARITY GENERA
FRAME BIT SYNCHRONIZER
STRESS GENERATOR
U36c 10102
U22b 10107
U25b 10231 C
U25a 10231 C
U16c 10107
U30a 10102
U23a 10106
U27a 10231 C
U24b 10102
U24c 10102
U24d 10102
U24a 10102
U20c 10103
U20b 10103
U20a 10103
U21a 10231 C
U21b 10231 C
U26 10016
U22c 10107
R100
R101
R39
R51
R105
R84
R86
R87
R88
R89
R91
R92 1K
R93
R94
R95
R96
R97
R98
R115
R121
R122
R124
R125 5.1K
R145
R80
R81
R82
R83
R90 1K
C16 .01
C17 .01
C18
C19
C20
C21
CR3 IN4148
DS IN4148
-5.2
RA 160
RA 270
RC 470
RESISTORS 1/10 W 5%

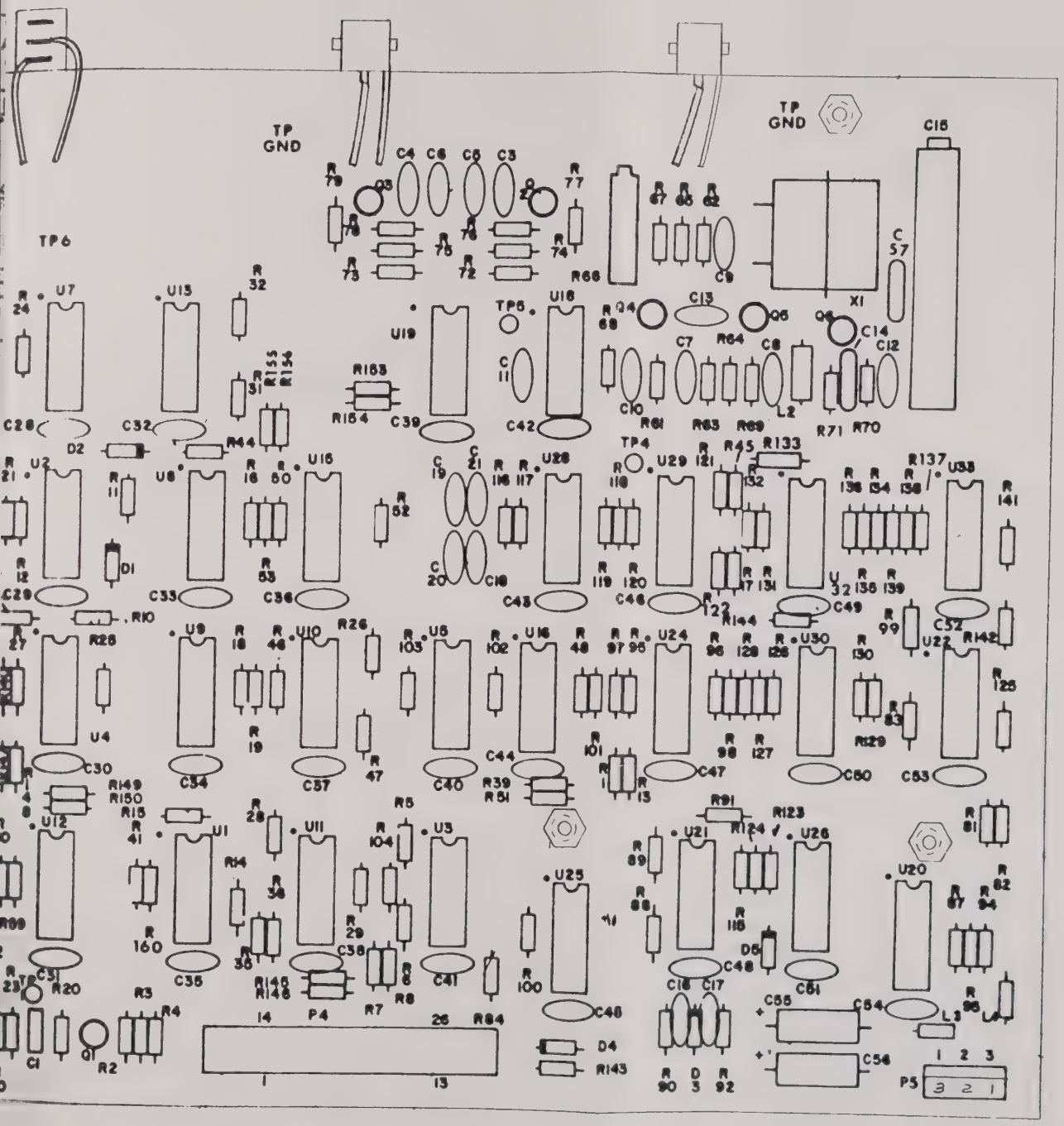


FT3 Test Set Transmitter (ECL)
Schematic (DFT3-101)

Fig. 5-3 Sheet 2

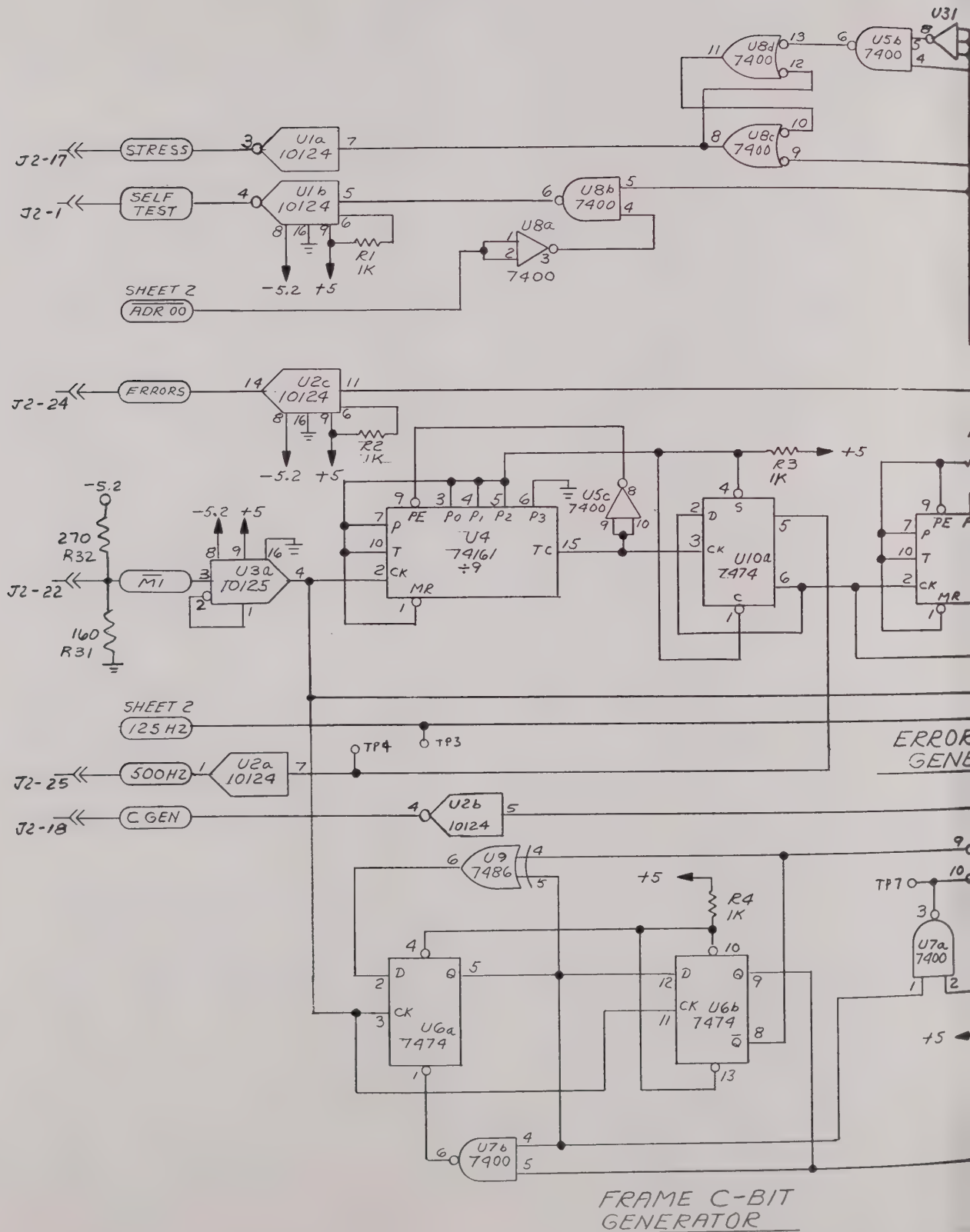


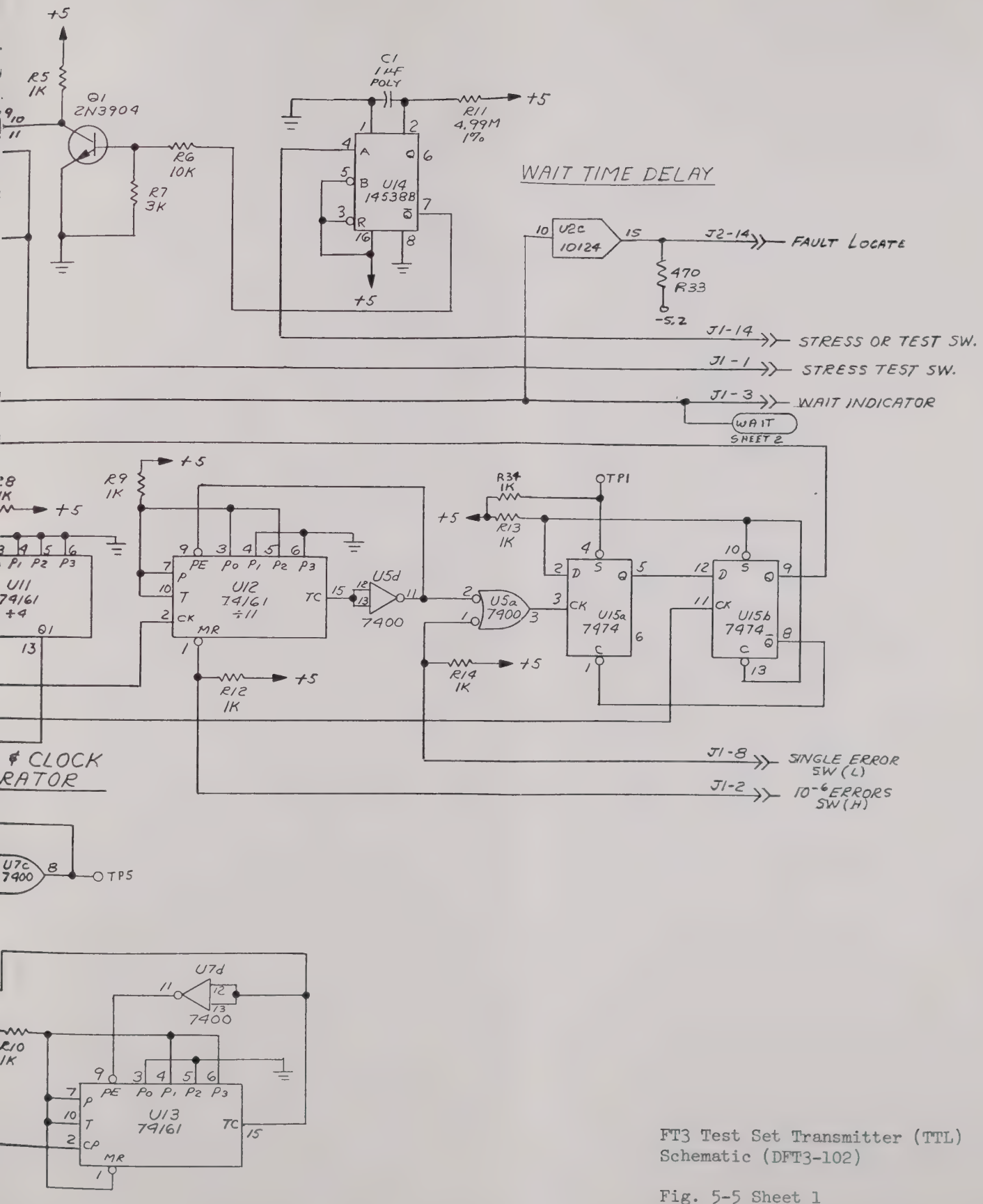

R109
U31
R 107
U6
R110
R 111
R 114
R 108
C22
R 105
C 25
R 112
R37
U 27
R 106
C 23
C 26
TP3
R80
U14
R 49
R 56
R 54
U17
R 58
R 55
R 57
C27
C24
R 151
R 152
L1



FT3 Transmitter (ECL) P.C. Board Assembly (DFT3-201)

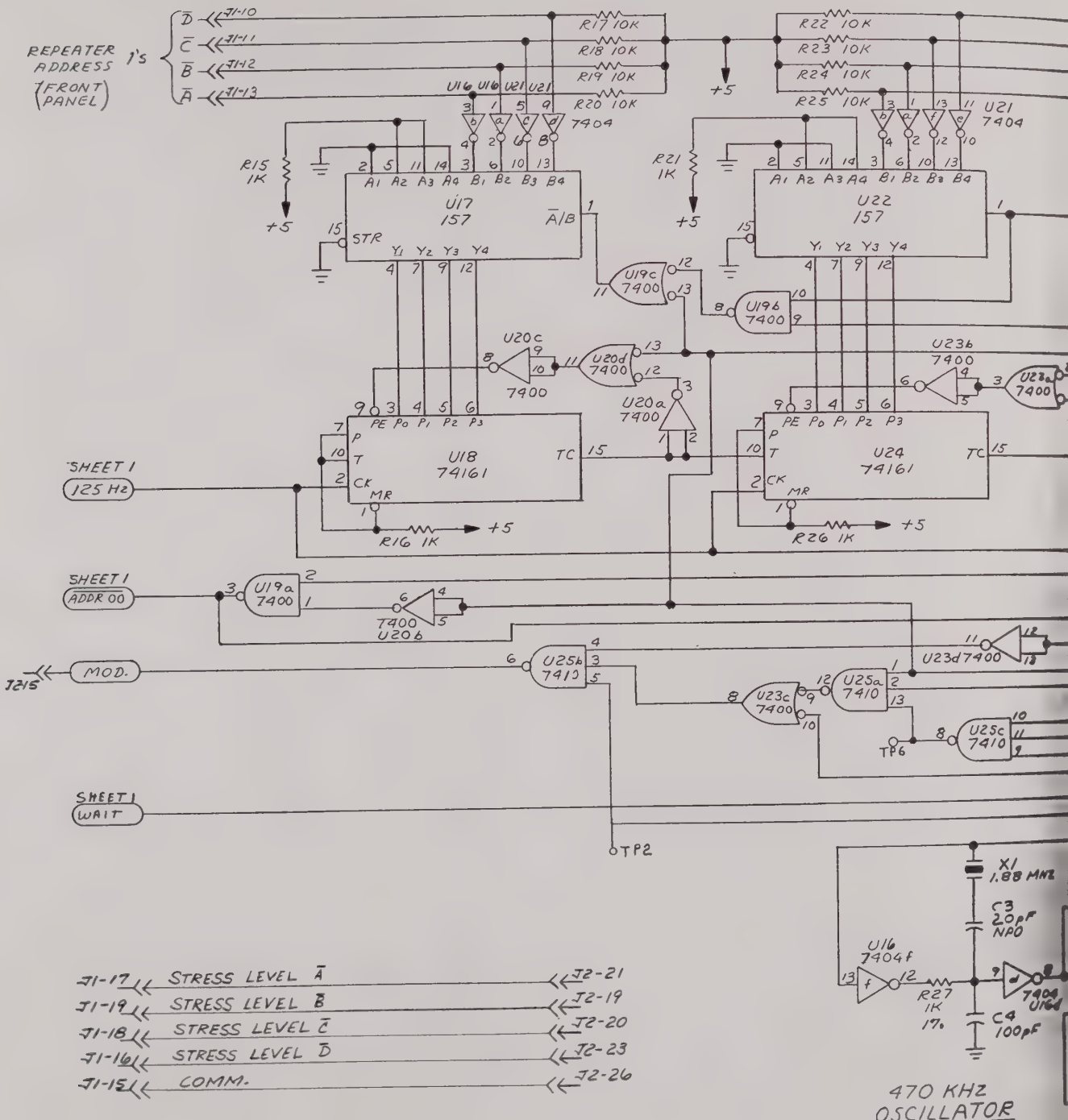
Fig. 5-4

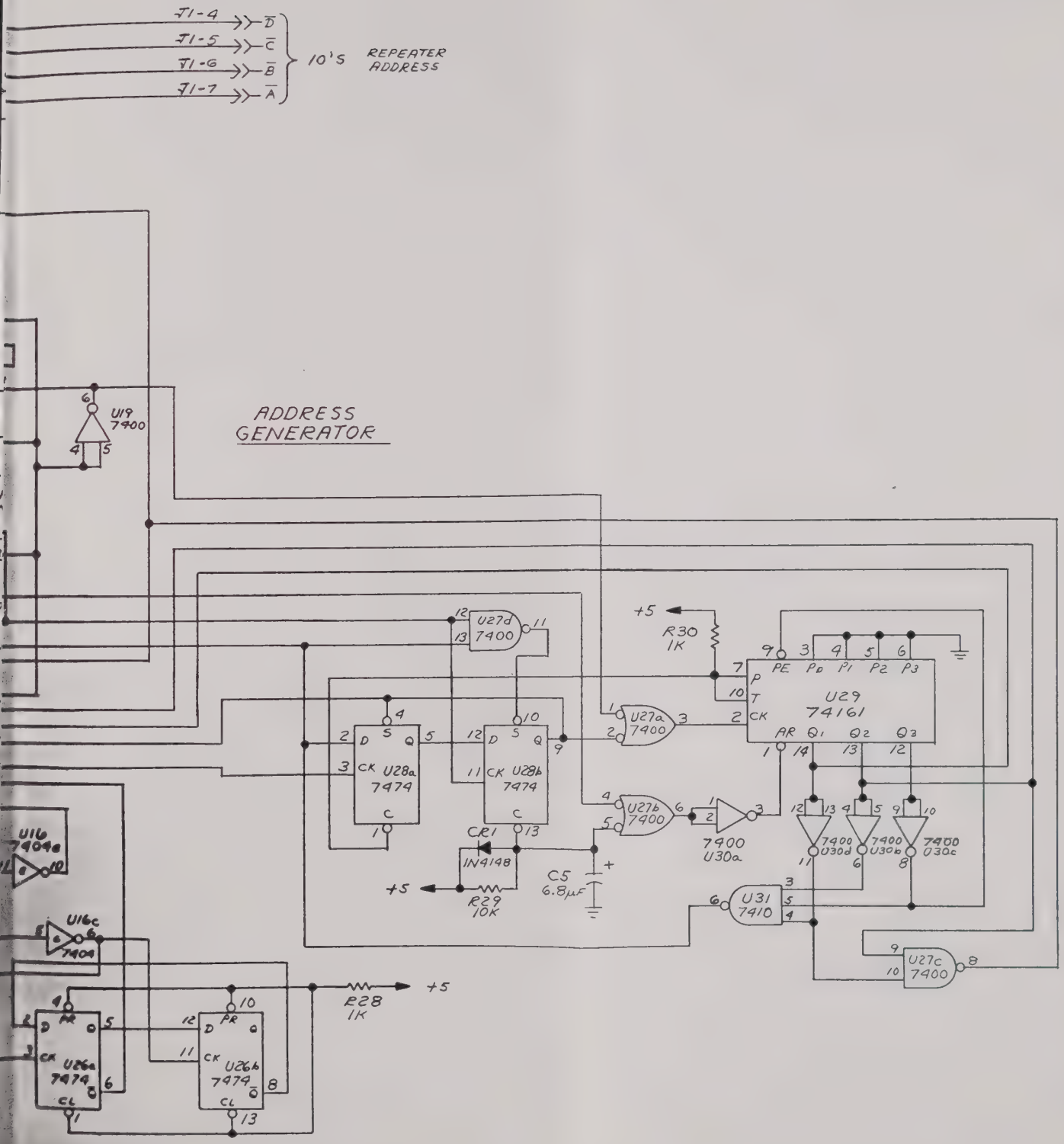

J2-17
STRESS
U1a 10124
J2-1
SELF TEST
U1b 10124
R1 1K
-5.2
+5
SHEET 2
ADR 00
U8a 7400
U8b 7400
U8c 7400
U8d 7400
U5b 7400
U31
J2-24
ERRORS
U2c 10124
R2 1K
R3 1K
U5c 7400
U4 74161 ÷9
PE
P0 P1 P2 P3
TC
U10a 7474
J2-22
M1
U3a 10125
270 R32
160 R31
SHEET 2
125 H2
J2-25
500H2
U2a 10124
TP4
TP3
J2-18
C GEN
U2b 10124
U9 7486
R4 1K
U6a 7474
U6b 7474
U7a 7400
U7b 7400
TP7
ERROR GENE
FRAME C-BIT GENERATOR



FT3 Test Set Transmitter (TTL)
Schematic (DFT3-102)

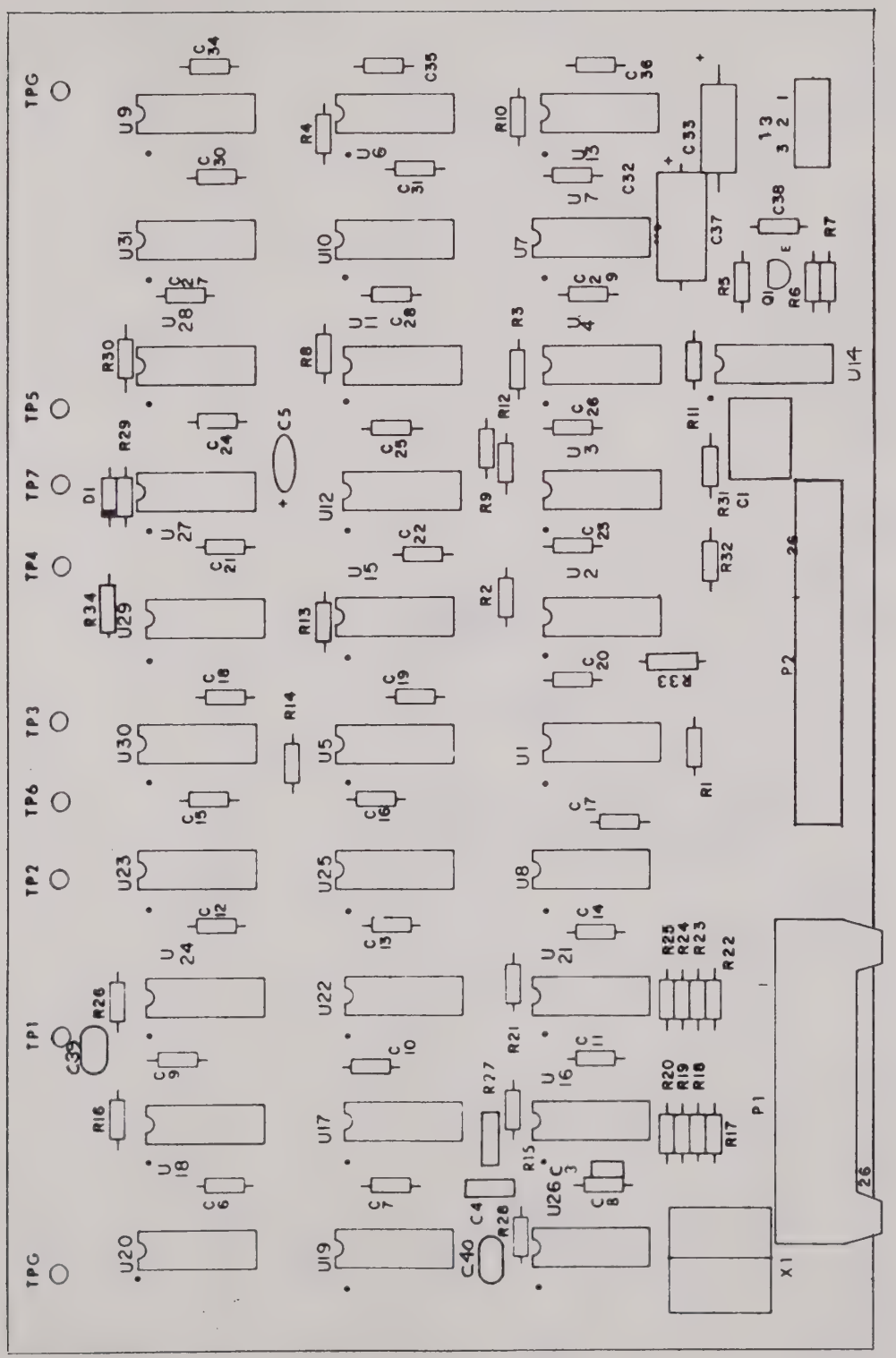
Fig. 5-5 Sheet 1


REPEATER ADDRESS J's (FRONT PANEL)
D J1-10
C J1-11
B J1-12
A J1-13
R17 10K
R18 10K
R19 10K
R20 10K
U16 U16 U21 U21
7404
+5
R22 10K
R23 10K
R24 10K
R25 10K
U21 7404
R15 1K
R21 1K
U17 157
U22 157
A/B
STR
Y1 Y2 Y3 Y4
A1 A2 A3 A4 B1 B2 B3 B4
U19c 7400
U19b 7400
U20c 7400
U20d 7400
U20a 7400
U23b 7400
U18 74161
U24 74161
PE P0 P1 P2 P3
TC
MR
R16 1K
R26 1K
SHEET 1
125 Hz
SHEET 1
ADDR 00
U19a 7400
U20b 7400
MOD.
J215
U25b 7410
U23d 7400
U23c 7400
U25a 7410
U25c 7410
TP6
SHEET 1
WAIT
TP2
J1-17 STRESS LEVEL A J2-21
J1-19 STRESS LEVEL B J2-19
J1-18 STRESS LEVEL C J2-20
J1-16 STRESS LEVEL D J2-23
J1-15 COMM. J2-26
X1 1.88 MHz
C3 20pF NPO
U16 7404f
R27 1K 1%
C4 100pF
7404 U16d
470 KHZ OSCILLATOR



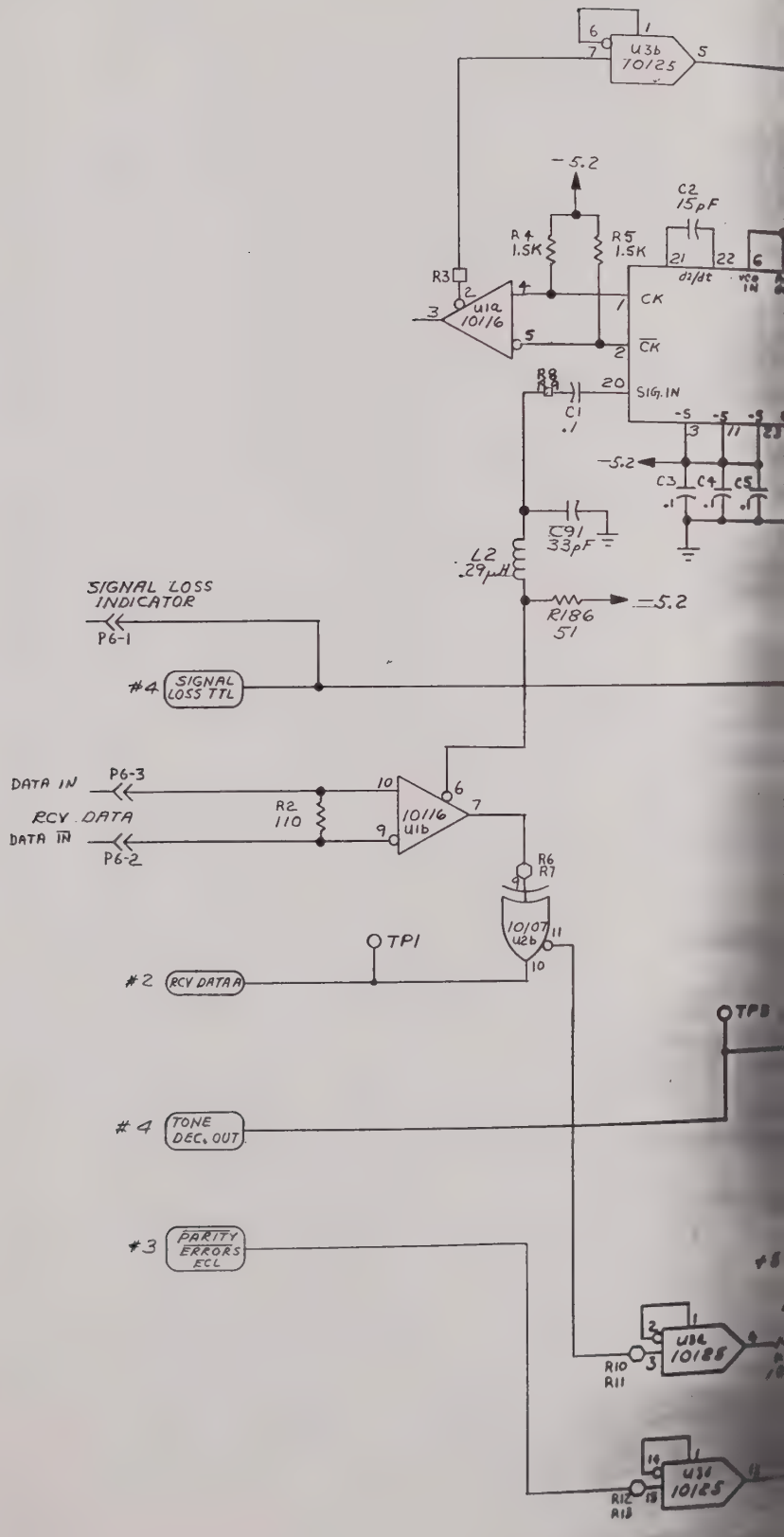
FT3 Test Set Transmitter (TTL)
Schematic (DFT3-102)

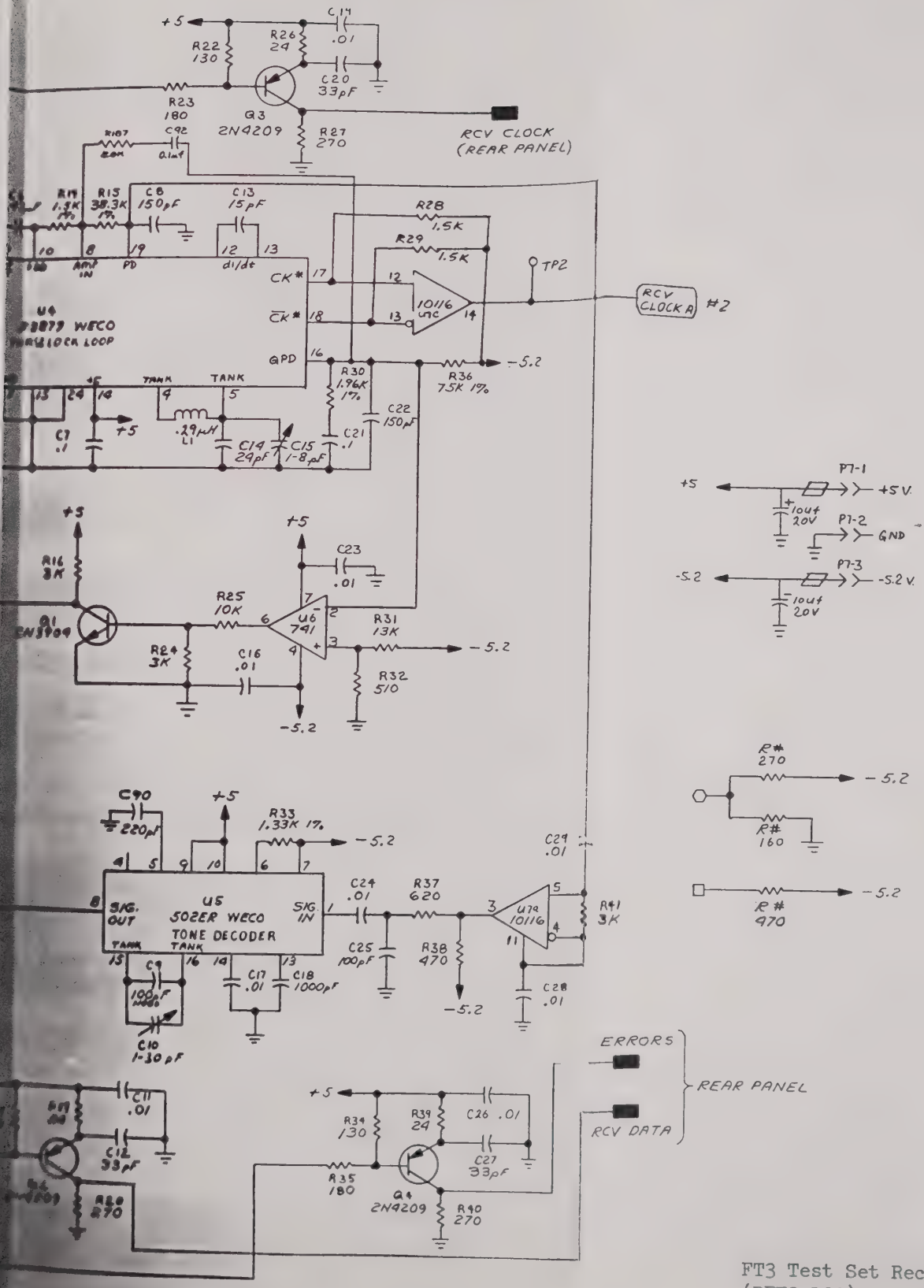
Fig. 5-5 Sheet 2



FT3 Transmitter (TTL) Board
Assembly (CFT3-202)

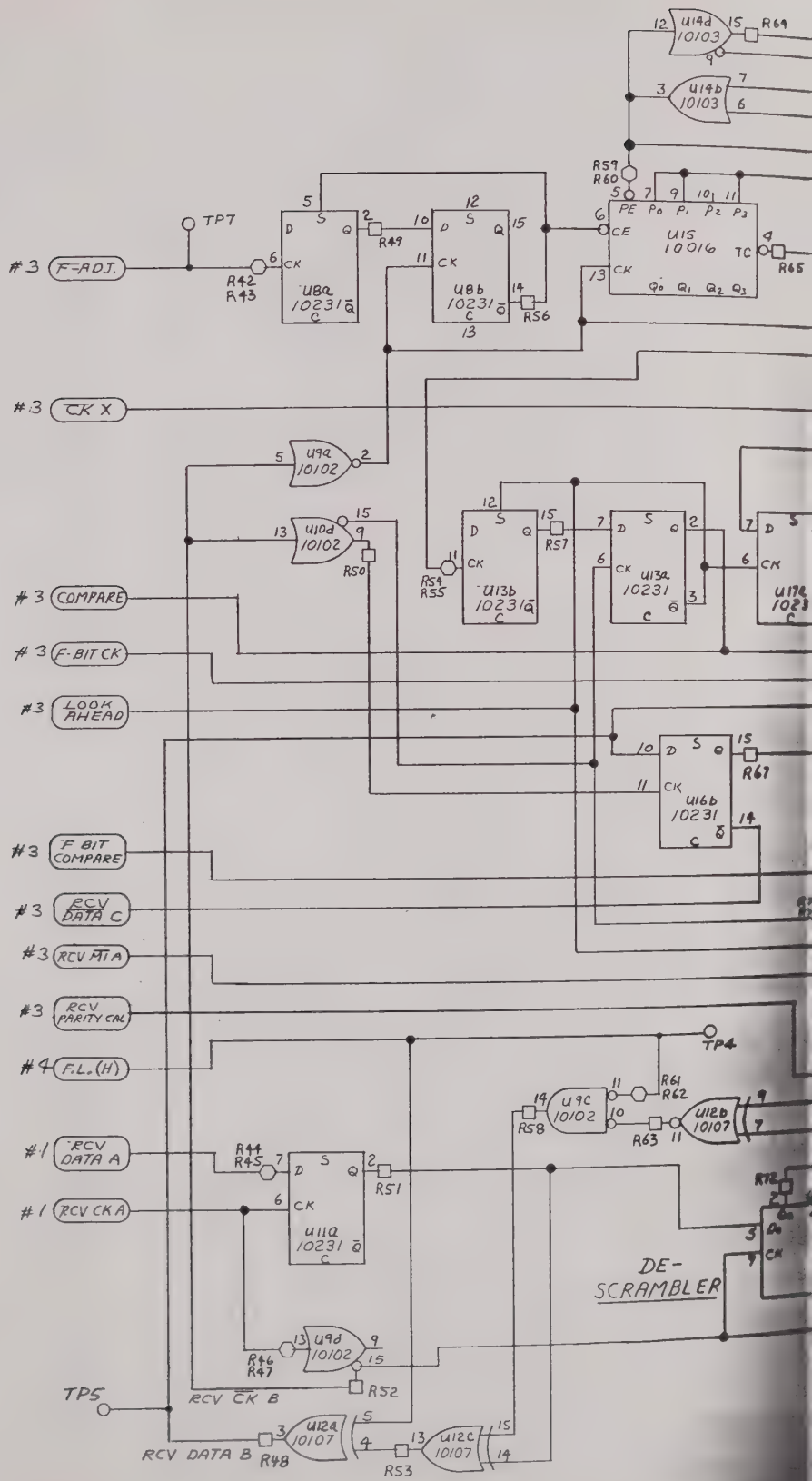
Fig. 5-6

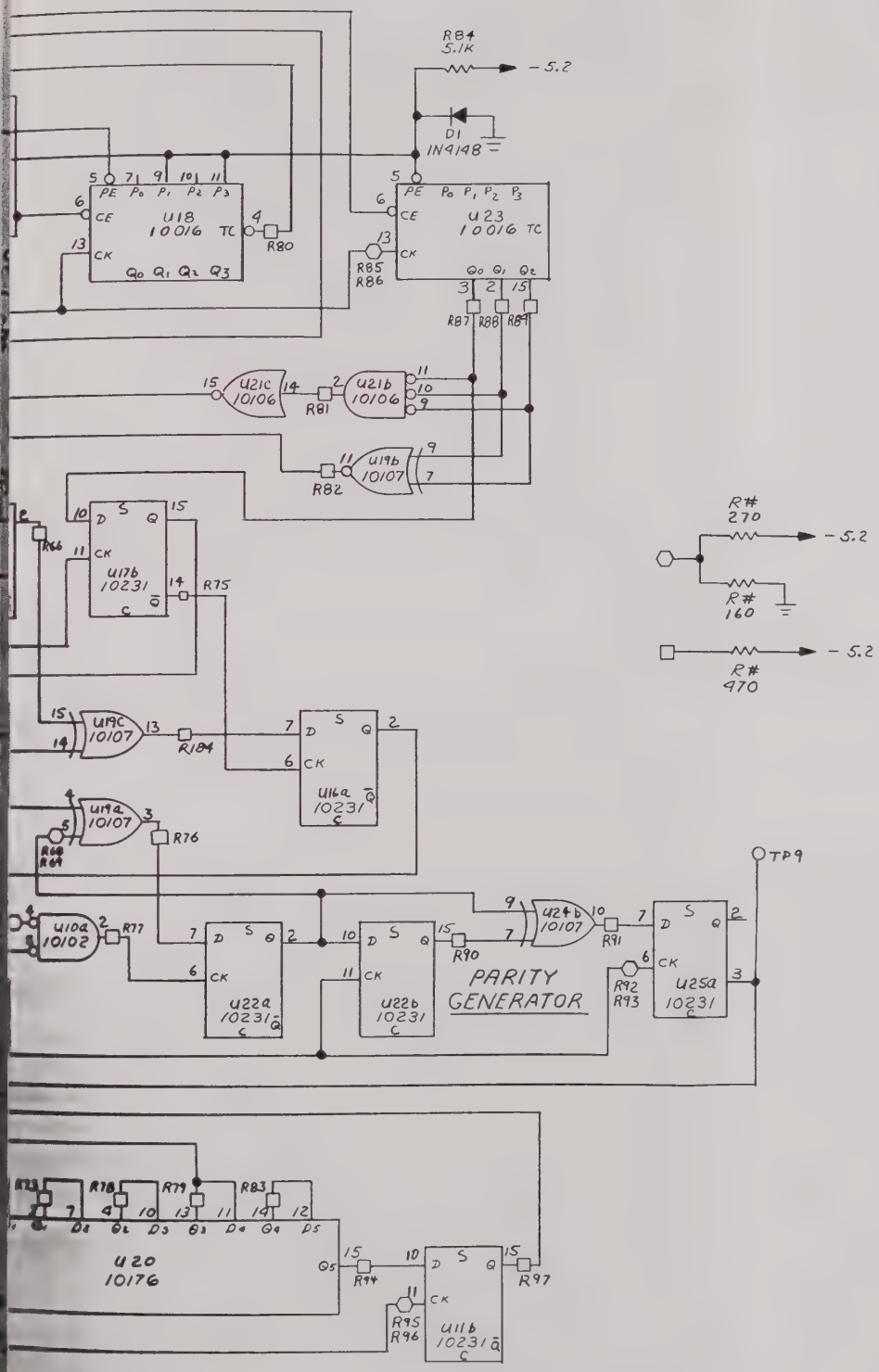

U3b
10125
-5.2
C2
15pF
R4
1.5K
R5
1.5K
R3
U1a
10116
CK
CK
SIG. IN
C1
.1
C3
C4
C5
C91
33pF
L2
.29μH
R186
51
SIGNAL LOSS
INDICATOR
P6-1
#4
SIGNAL
LOSS TTL
DATA IN
P6-3
RCV DATA
DATA IN
P6-2
R2
110
10116
U1b
R6
R7
10107
U2b
TP1
#2
RCV DATA A
TP8
#4
TONE
DEC. OUT
#3
PARITY
ERRORS
ECL
U1c
10125
R10
R11
U3c
10125
R12
R13



FT3 Test Set Receiver Schematic (DFT3-103)

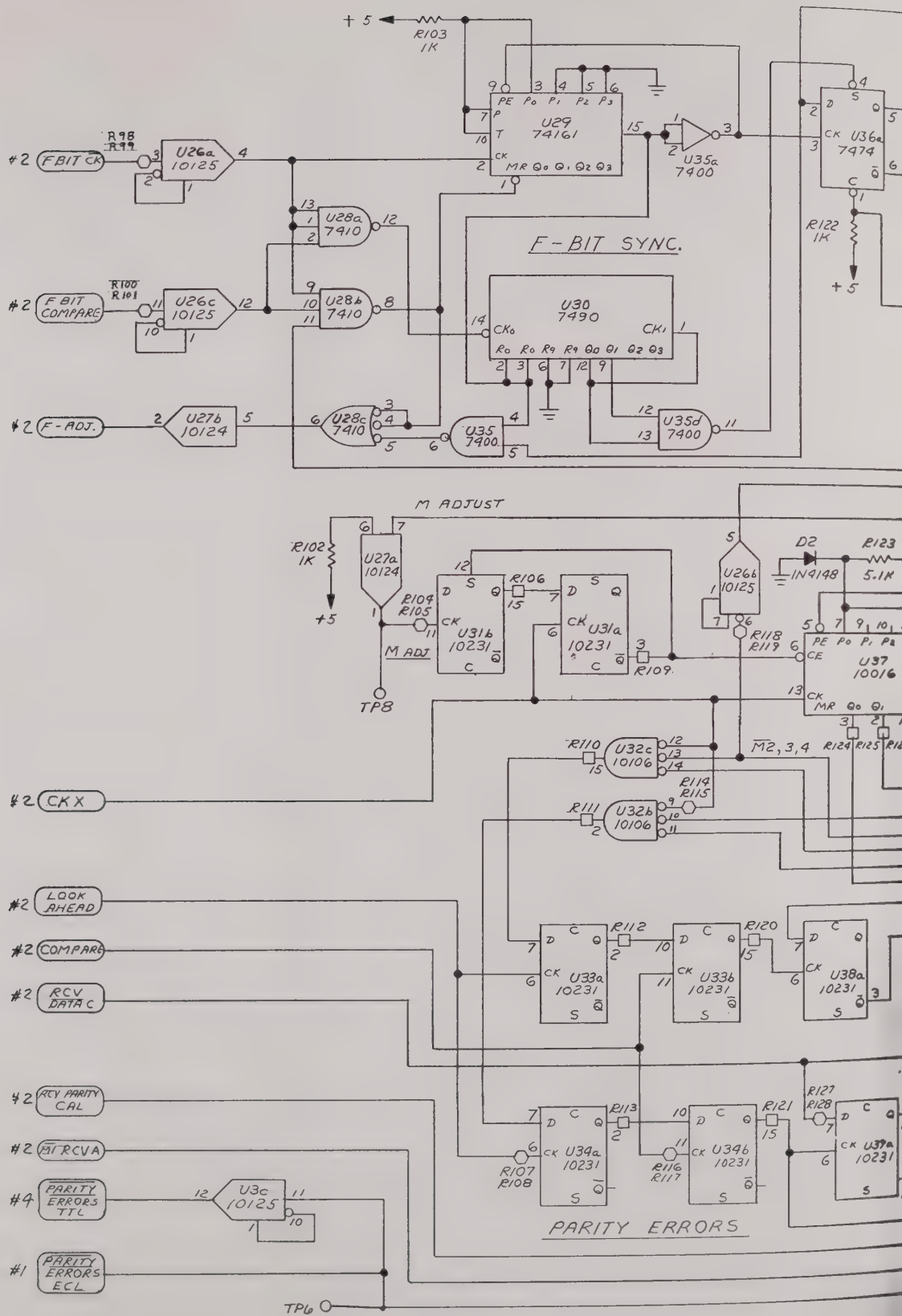
Fig. 5-7 Sheet 1

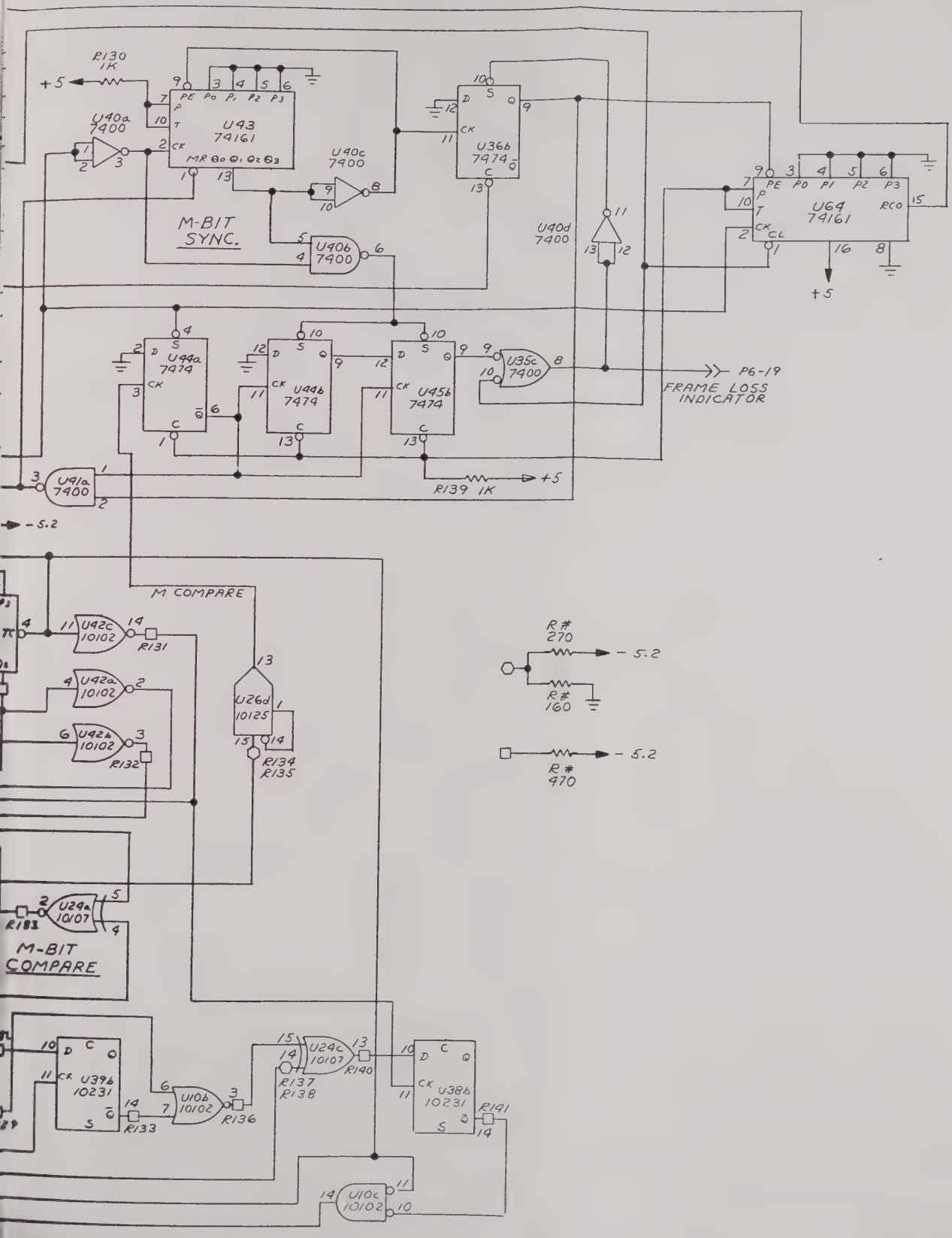

#3 F-ADJ.
TP7
R42
R43
U8a 10231 C
R49
U8b 10231 C
R56
U14d 10103
R69
U14b 10103
R59
R60
U15 10016
R65
#3 CK X
U9a 10102
U10d 10102
R50
U13b 10231 C
R54
R55
R57
U13a 10231 C
#3 COMPARE
#3 F-BIT CK
#3 LOOK AHEAD
U16b 10231 C
R67
#3 F BIT COMPARE
#3 RCV DATA C
#3 RCV DATA A
#3 RCV PARITY CAL
#4 F.L.(H)
TP4
U9c 10102
R58
R61
R62
R63
U12b 10107
#1 RCV DATA A
#1 RCV CK A
R44
R45
U11a 10231 C
R51
DE-SCRAMBLER
U9d 10102
R46
R47
TP5
RCV CK B
R52
RCV DATA B
R48
U12a 10107
U12c 10107
R53



FT3 Test Set Receiver Schematic
(DFT3-103)

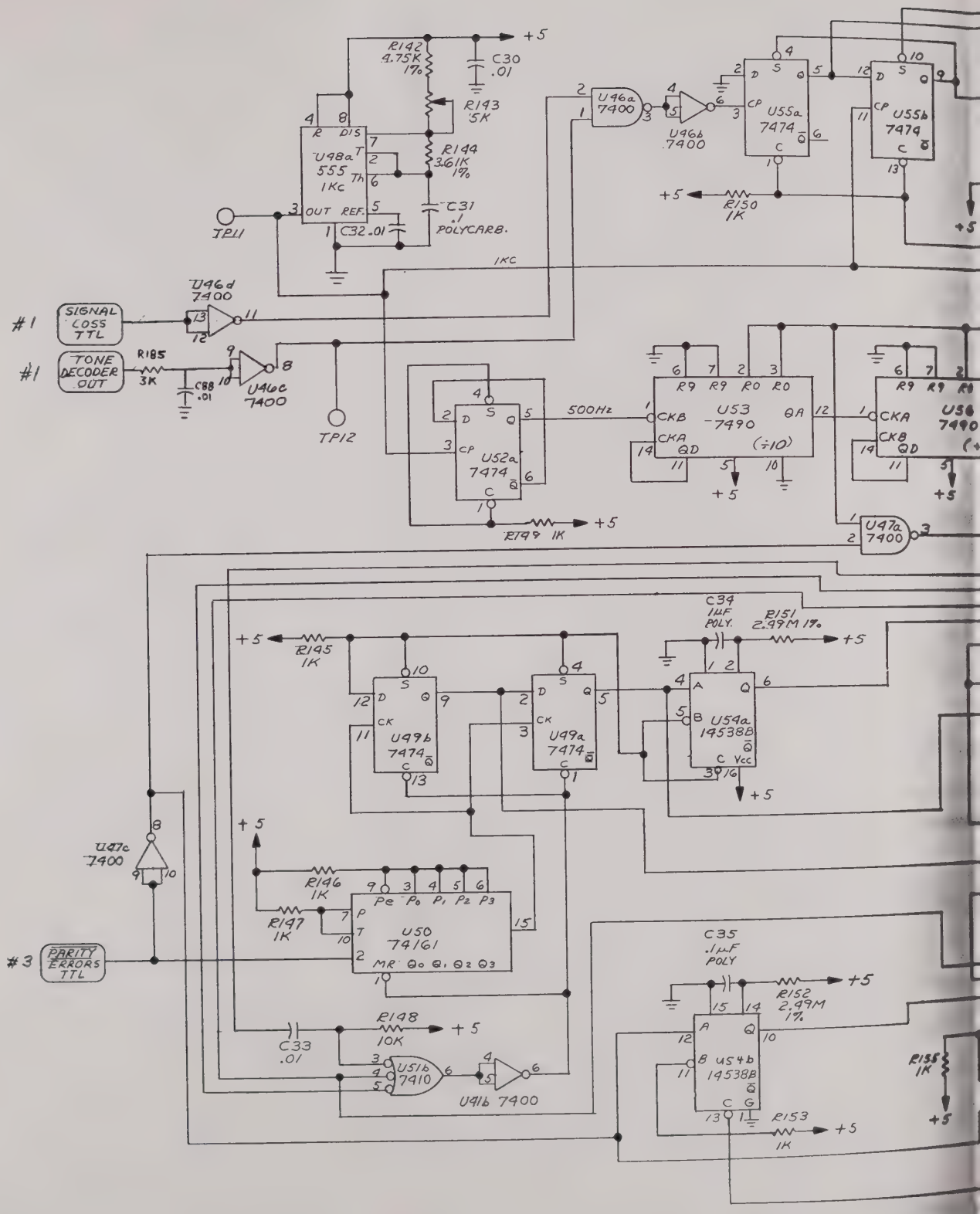
Fig. 5-7 Sheet 2

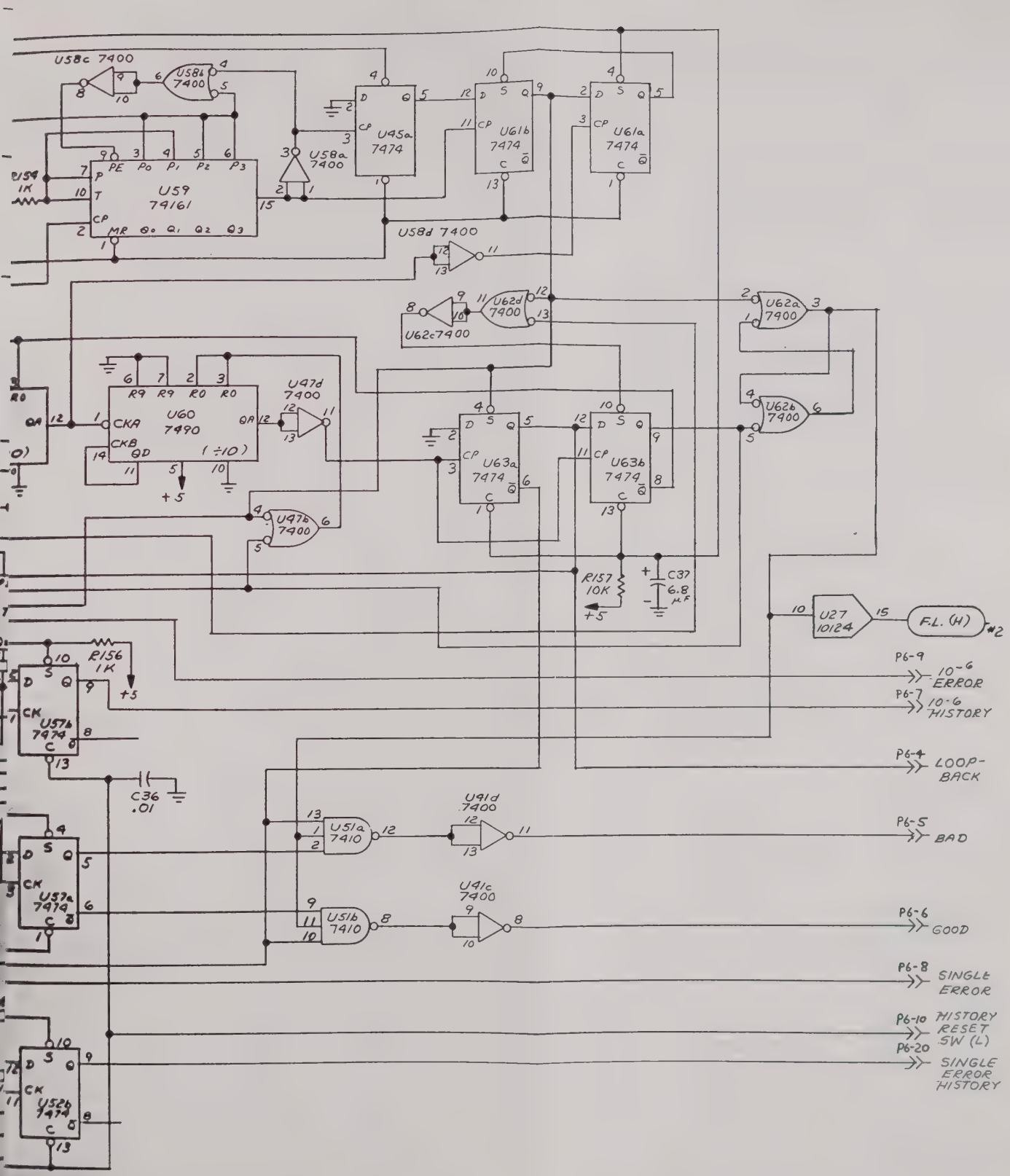

+5
R103 1K
U29 74161
U35a 7400
U36a 7474
R122 1K
#2 FBIT CK
R98 R99
U26a 10125
U28a 7410
F-BIT SYNC.
#2 F BIT COMPARE
R100 R101
U26c 10125
U28b 7410
U30 7490
#2 F-ADJ.
U27b 10124
U28c 7410
U35 7400
U35d 7400
M ADJUST
R102 1K
U27a 10124
R104 R105
M ADJ
TP8
U31b 10231
R106
U31a 10231
R109
U26b 10125
D2 IN4148
R123 5.1K
R118 R119
U37 10016
R110
U32c 10106
R114 R115
R111
U32b 10106
M2,3,4
R124 R125
#2 CK X
#2 LOOK AHEAD
#2 COMPARE
#2 RCV DATA C
U33a 10231
R112
U33b 10231
R120
U38a 10231
#2 RCV PARITY CAL
#2 M1 RCVA
#4 PARITY ERRORS TTL
U3c 10125
#1 PARITY ERRORS ECL
R107 R108
U39a 10231
R113
R116 R117
U39b 10231
R121
R127 R128
U37a 10231
PARITY ERRORS
TP6



FT3 Test Set Receiver Schematic (DFT3-103)

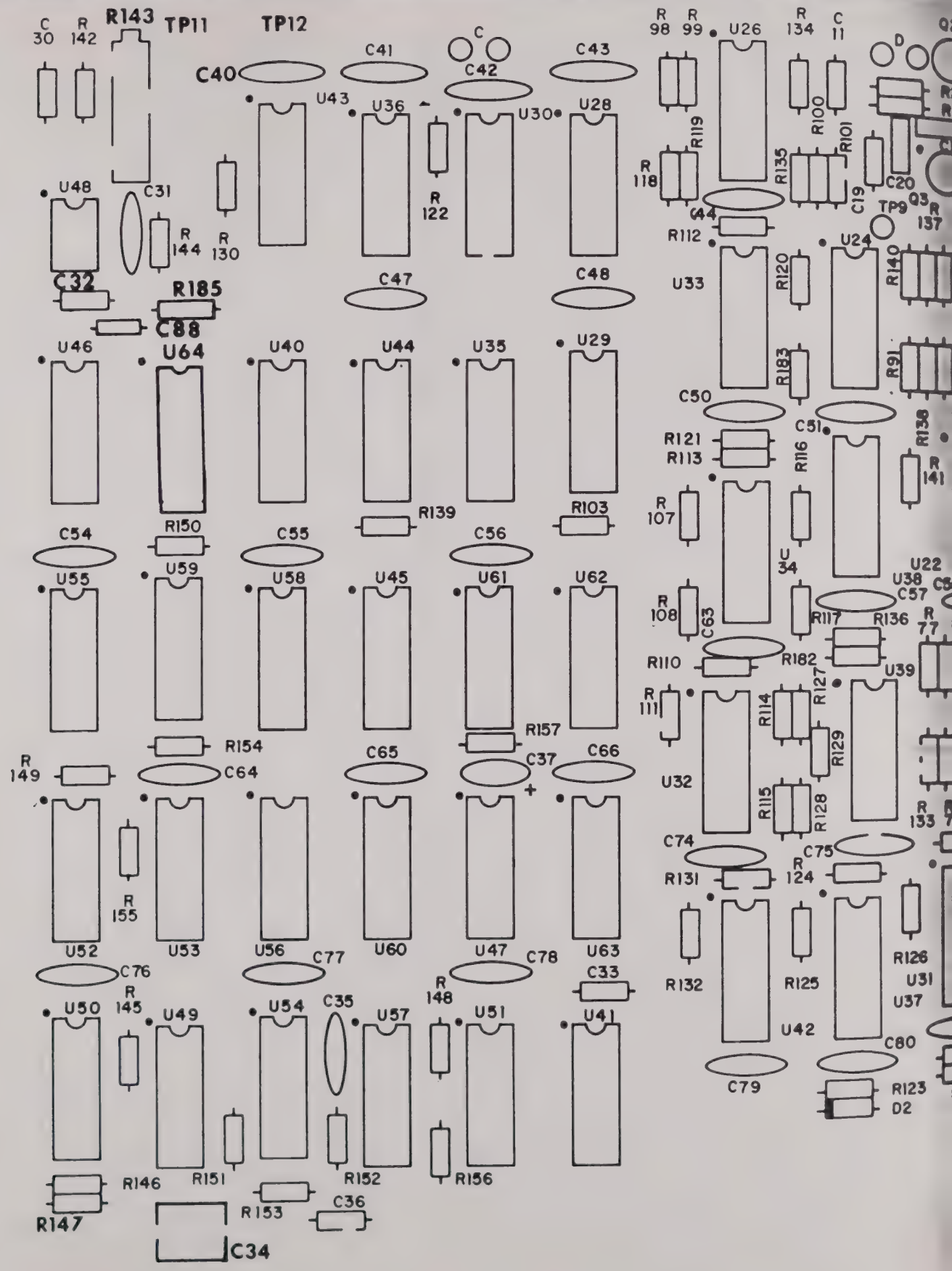
Fig. 5-7 Sheet 3

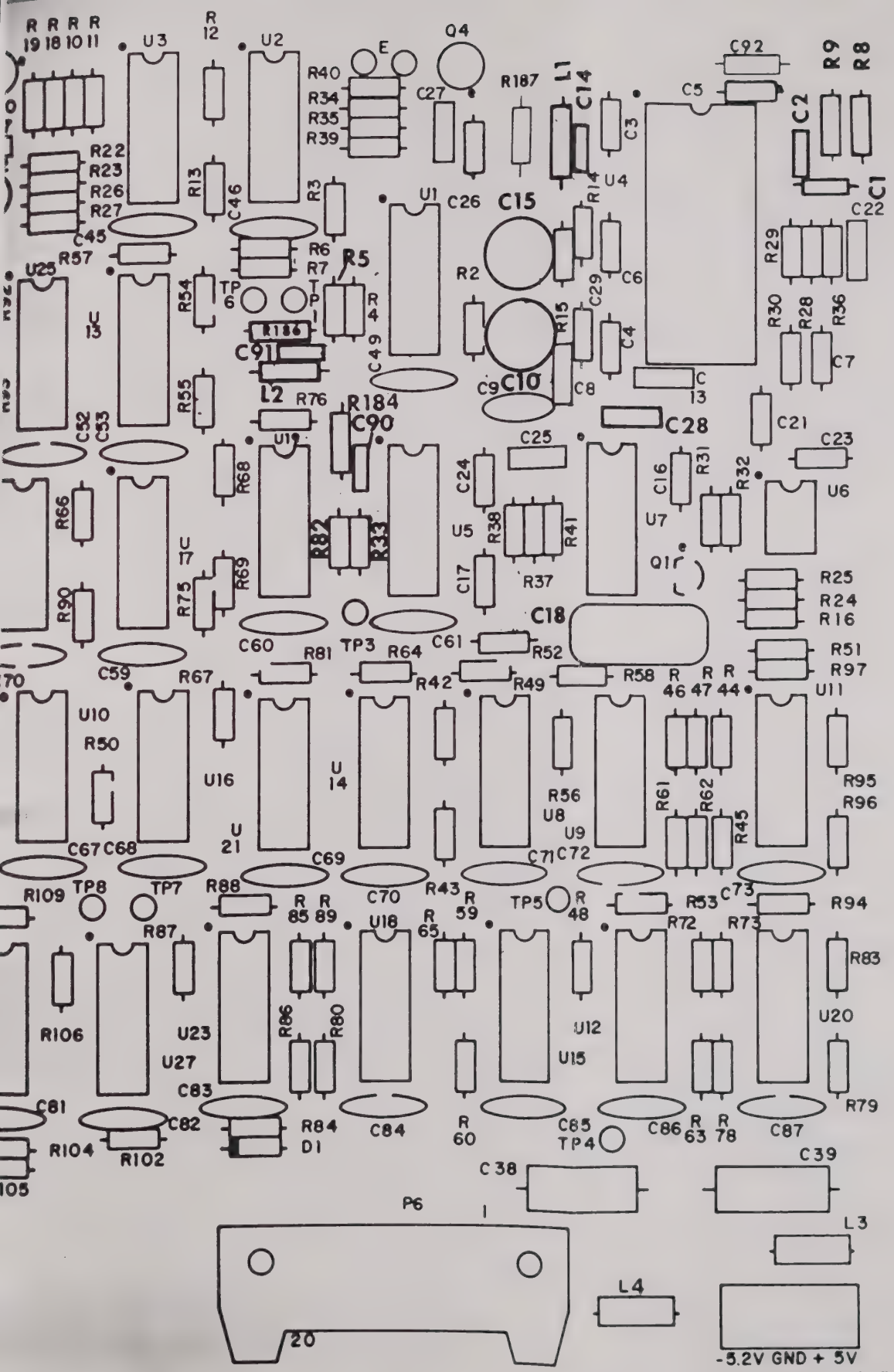

R142 4.75K 1%
C30 .01
+5
R143 5K
R144 3.61K 1%
U98a 555 1Kc
C31 .1 POLYCARB.
C32 .01
TP11
1KC
U46a 7400
U46b 7400
U55a 7474
U55b 7474
R150 1K
#1 SIGNAL LOSS TTL
#1 TONE DECODER OUT
R185 3K
C88 .01
U46d 7400
U46c 7400
TP12
U52a 7474
500Hz
U53 7490 (÷10)
R149 1K
U47a 7400
C34 1μF POLY.
R151 2.99M 1%
R145 1K
U49b 7474
U49a 7474
U54a 14538B
U47c 7400
R146 1K
R147 1K
U50 74161
#3 PARITY ERRORS TTL
C33 .01
R148 10K
U51b 7410
U49b 7400
C35 .1μF POLY
R152 2.99M 1%
U54b 14538B
R153 1K
R135 1K



FT3 Test Set Receiver Schematic
(DFT3-103)

Fig. 5-7 Sheet 4

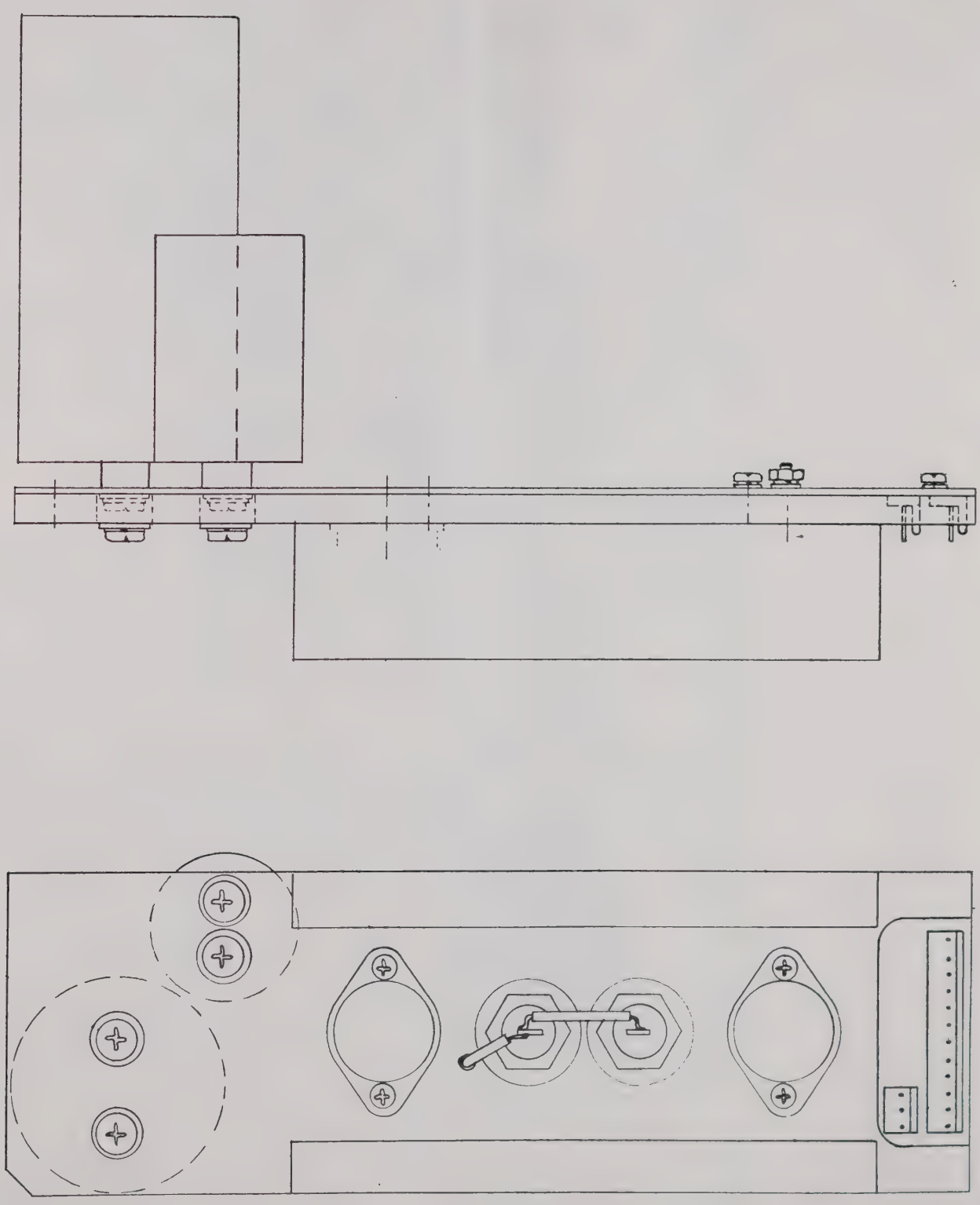

C 30
R 142
R143
TP11
TP12
C40
C41
C
C42
C43
U43
U36
U30
U28
R 130
R 122
U48
C31
R 144
C32
R185
C88
C47
C48
U46
U64
U40
U44
U35
U29
R139
R103
C54
R150
C55
C56
U55
U59
U58
U45
U61
U62
R154
R157
R 149
C64
C65
C37
C66
U52
U53
U56
U60
U47
U63
R 155
C76
C77
C78
C33
R 145
R 148
U50
U49
U54
C35
U57
U51
U41
R146
R151
R152
R156
R147
R153
C36
C34
R 98
R 99
U26
R 134
C 11
D
R119
R100
R101
R 118
R135
C19
C20
TP9
Q3
R 137
C44
R112
U24
U33
R120
R140
R183
R91
C50
C51
R138
R121
R113
R116
R 141
R 107
C34
U22
U38
C57
R 108
C63
R117
R136
R 77
R110
R182
U39
R 111
R114
R127
R129
U32
R115
R128
R 133
C74
C75
R131
R 124
R126
R132
R125
U31
U37
U42
C80
C79
R123
D2



FT3 Receiver P.C. Board Assembly
(DFT3-203)

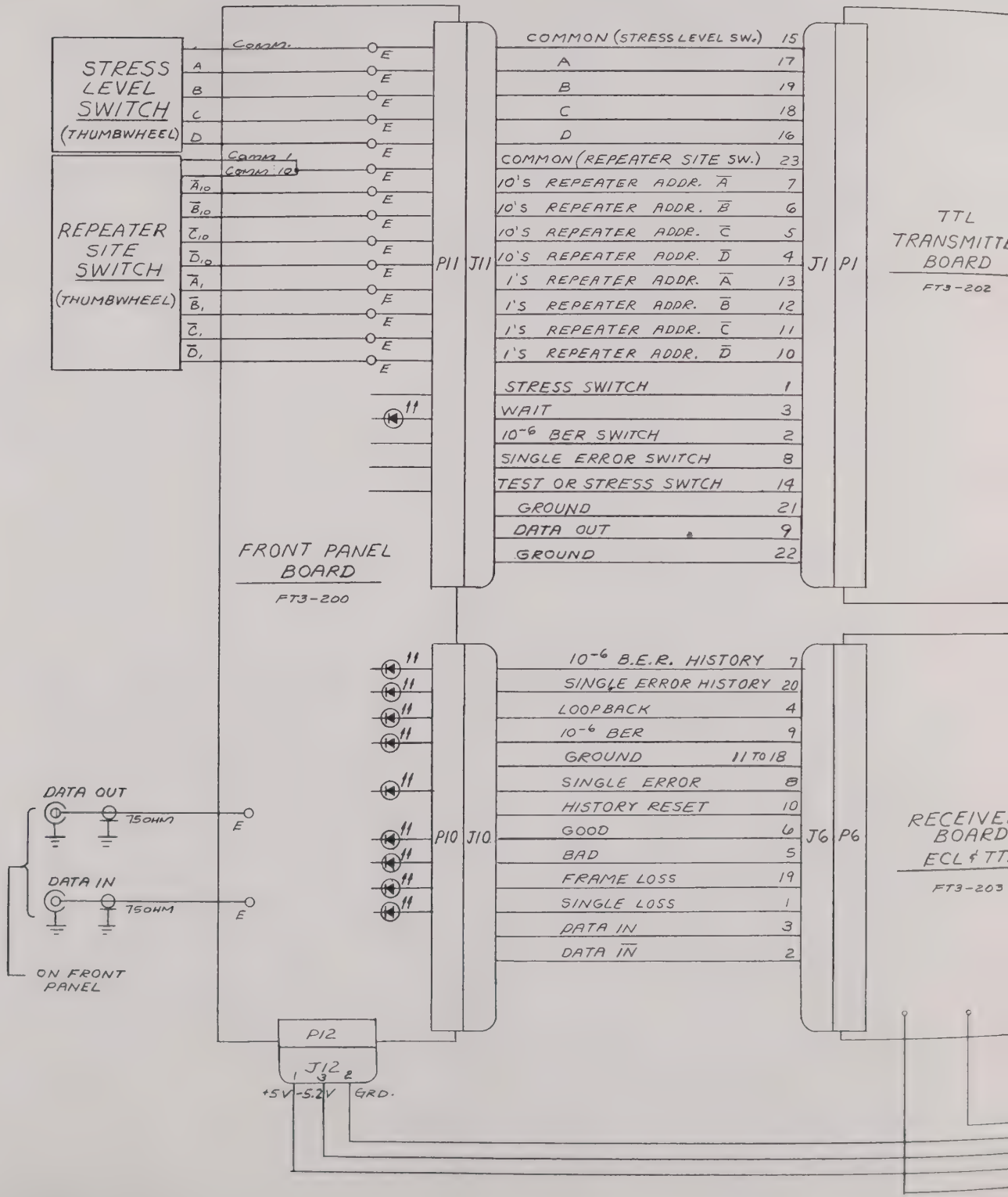
FT3 Test Set Power Supply Schematic (CFT3-104)

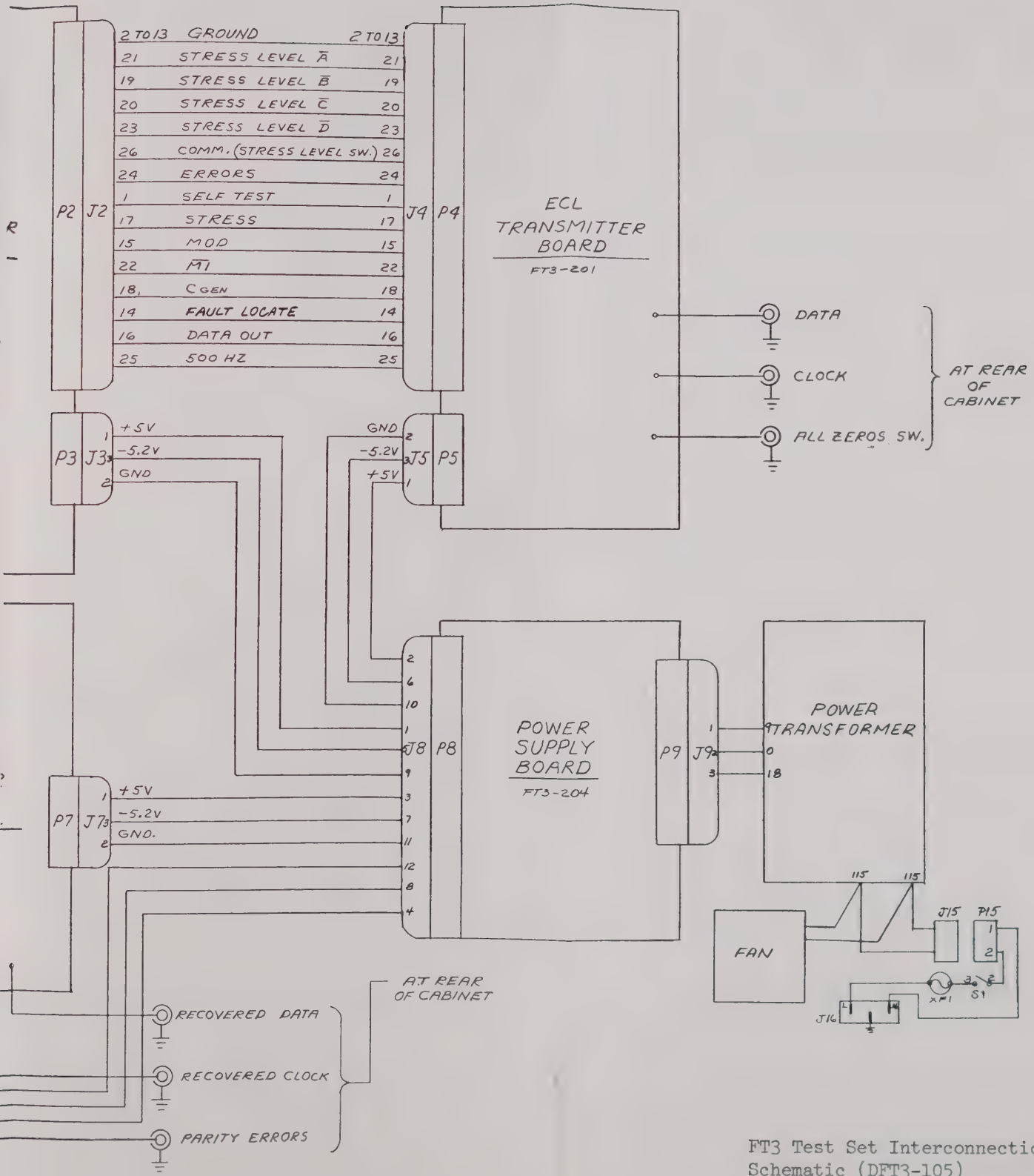
Fig. 5-9



FT3 Power Supply Assembly
(CFT3-207)

Fig. 5-10


STRESS LEVEL SWITCH (THUMBWHEEL)
REPEATER SITE SWITCH (THUMBWHEEL)
COMM.
A
B
C
D
COMM 1
COMM 10
$\overline{A}_{10}$
$\overline{B}_{10}$
$\overline{C}_{10}$
$\overline{D}_{10}$
$\overline{A}_1$
$\overline{B}_1$
$\overline{C}_1$
$\overline{D}_1$
E
11
P11 J11
FRONT PANEL BOARD
FT3-200
COMMON (STRESS LEVEL SW.) 15
A 17
B 19
C 18
D 16
COMMON (REPEATER SITE SW.) 23
10'S REPEATER ADDR. $\overline{A}$ 7
10'S REPEATER ADDR. $\overline{B}$ 6
10'S REPEATER ADDR. $\overline{C}$ 5
10'S REPEATER ADDR. $\overline{D}$ 4
1'S REPEATER ADDR. $\overline{A}$ 13
1'S REPEATER ADDR. $\overline{B}$ 12
1'S REPEATER ADDR. $\overline{C}$ 11
1'S REPEATER ADDR. $\overline{D}$ 10
STRESS SWITCH 1
WAIT 3
10^{-6} BER SWITCH 2
SINGLE ERROR SWITCH 8
TEST OR STRESS SWTCH 14
GROUND 21
DATA OUT 9
GROUND 22
J1 P1
TTL TRANSMITTE BOARD
FT3-202
P10 J10
10^{-6} B.E.R. HISTORY 7
SINGLE ERROR HISTORY 20
LOOPBACK 4
10^{-6} BER 9
GROUND 11 TO 18
SINGLE ERROR 8
HISTORY RESET 10
GOOD 6
BAD 5
FRAME LOSS 19
SINGLE LOSS 1
DATA IN 3
DATA $\overline{IN}$ 2
J6 P6
RECEIVE BOARD ECL & TT
FT3-203
DATA OUT
75OHM
DATA IN
75OHM
ON FRONT PANEL
P12
J12
1 3 2
+5V -5.2V GRD.



FT3 Test Set Interconnection Schematic (DFT3-105)

Fig. 5-11

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 DISPLAY BOARD P.C. ASSEMBLY			
R1 - R10	Resistor, 200 ohm, 1/4W, 5%		RCR07G201JS
R11,13,14,15,16, R17,18,19,20,32, R34	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R12	Resistor, 100 ohm, 1/4W, 5%		RCR07G101JS
R21	Resistor, 200 ohm, 1/4W, 5%		RCR07G201JS
R22	Resistor, 130 ohm, 1/4W, 5%		RCR07G131JS
R23, 44	Resistor, 270 ohm, 1/4W, 5%		RCR07G271JS
R24, 29	Resistor, 470 ohm, 1/4W, 5%		RCR07G471JS
R25	Resistor, 47 ohm, 1/4W, 5%		RCR07G470JS
R26, 28	Resistor, 150 ohm, 1/4W, 5%		RCR07G151JS
R27	Resistor, 62 ohm, 1/4W, 5%		RCR07G620JS
R30	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R31	Resistor, 8.2M, 1/10W, 1%		RCR07G825JS
R33, 38, 41	Resistor, 3K, 1/4W, 5%		RCR07G302JS
R35,36,39,42	Resistor, 510 ohm, 1/4W, 5%		RCR07G511JS
C1, C4, C6	Capacitor, .1uf, 50V	Unitrode	CGD104ZDZ
C2,C3,C9,C10 & 8 Places Marked "C"	Capacitor, .01uf, 50V	Unitrode	CGC103ZDZ
C5, C7	Capacitor, 10uf, 20V, Tant.	Sprague	196D106X9020JA1
C8	Capacitor, 1uf, Polycarb	Siemens	B32561-1-5-100
Q1	Transistor		2N2369
Q2	Transistor		2N4209
Q3, Q4, Q5	Transistor		2N3904
U1, U2, U8	Integrated Circuit		SN7400N
U3	Integrated Circuit		SN7403N
U4, U5	Integrated Circuit		SN7405N
U6	Integrated Circuit	Motorola, Fairchild or Signetics	MC10116P or F10116PC
U7	Integrated Circuit	Motorola	MC14538BPC
DS1,2,3,4,7,8,9	Diode, L.E.D. (Red)	H/P	5082-4650
DS5, DS10	Diode, L.E.D. (Yellow)	H/P	5082-4550
DS6	Diode, L.E.D. (Green)	H/P	5082-4950
S1,2,3,4,5	Switch, Push Button With Cap	C & K	8125-V30 (Small Black (2) Cap)
R43	Resistor, 160, 1/4W, 5%		RCR07G161JS
P11	Connector, 26 Pin	3M	3429-1002
P10	Connector, 20 Pin	3M	3428-1002
P12	Connector, 3 Pin	Amp	640389-3

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 TRANSMITTER (ECL) P.C. BOARD ASSEMBLY			
P4	Connector (Straight)	3M	3429-2002
P5	Connector (3 Pin)	Amp	640388-3
R2	Resistor, 3K, 1/4W, 5%		RCR07G302JS
R11, R44, R123	Resistor, 5.1K, 1/4W, 5%		RCR07G512JS
R12,14,15,16,18,19, R21,22,24,25,26,27, R28,29,41,42,43,46, R47,48,49,50,52,53, R54,55,56,57,58,59, R60,62,70,83,84,86, R87,95,96,97,98,100, R101,102,103,104,105, R106,107,108,113,114, R115,116,117,118,119, R120,124,125,126,127, R128,129,91,130,131, R132,133,134,135,136, R137,138,139,99,140, R144,157,160	Resistor, 470 ohm, 1/4W, 5%		RCR07G471JS
R20	Resistor, 6.19K, 1/10W, 1%		RN55C6191F
R23, R63	Resistor, 3.9K, 1/4W, 5%		RCR07G392JS
R30	Resistor, 1.3K, 1/4W, 5%		RCR07G132JS
R64, R61	Resistor, 240 ohm, 1/4W, 5%		RCR07G241JS
R69, R71	Resistor, 22 ohm, 1/4W, 5%		RCR07G220JS
R68	Resistor, 2.2K, 1/4W, 5%		RCR07G222JS
R65	Resistor, 2K, 1/4W, 5%		RCR07G202JS
R67	Resistor, 680 ohm, 1/4W, 5%		RCR07G681JS
R1,5,8,10,45,32,34, R35,37,39,40,72,73, R82,88,94,110,112, R121,146,147,150, R151,153,141,155	Resistor, 160 ohm, 1/4W, 5%		RCR07G161JS
R75	Resistor, 130 ohm, 1/4W, 5%		RCR07G131JS
R76, R78	Resistor, 24 ohm, 1/4W, 5%		RCR07G240JS
R74	Resistor, 180 ohm, 1/4W, 5%		RCR07G181JS

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 TRANSMITTER (ECL) P.C. BOARD ASSEMBLY (Con't)			
R6,7,9,13,17,31,33, R36,38,51,77,79,80, R81,89,93,109,111, R122,145,148,149, R152,154,142, 156	Resistor, 270 ohm, 1/4W, 5%		RCR07G271JS
R4,92,90,143	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R3	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R66	Resistor, Var. 500 ohm, 2W	Helitrim	89W500
C55, C56	Capacitor, 10uf, 16V, EL	Capar	CAE-E10M16V
C3,4,C7 - C13 C16 - C54	Capacitor, .01uf, 50V	Unitrode	CGC103ZDZ
C2	Capacitor, S.M. 36 pf		CM04ED360J03
C1	Capacitor, S.M 220pf		CM05FD221J03
C6	Capacitor, S.M. 33pf		CM04ED330J03
C15	Capacitor Var. 1-30pf	Sprague	GGC-30000
X1	Crystal, 44.736 MHz	International Crystal	471540
D1,2,3,4,5	Diode		1N4148
Q4, Q5, Q6	Transistor		2N2369A
Q2, Q3	Transistor		2N4209
Q1	Transistor		2N3906
U1,4,3,6,28,24	Integrated Circuit	Motorola, Fairchild or Signetics	MC10102P or F10102PC
U8, U11	Integrated Circuit	Motorola, Fairchild or Signetics	MC10109P or F10109PC
U10,14,16,22	Integrated Circuit	Motorola, Fairchild or Signetics	MC10107P or F10107PC
U2,7,13,15,26	Integrated Circuit	Motorola, Fairchild or Signetics	F10016PC
U5,9,12,31,21,25,27	Integrated Circuit	Motorola, Fairchild or Signetics	MC10231P or F10231PC
U17,33,32,30	Integrated Circuit	Motorola, Fairchild or Signetics	MC10176P or F10176PC
U19	Integrated Circuit	Motorola, Fairchild or Signetics	MC10125P or F10125PC
C57	Capacitor, 15 pf, Sil. Mica		CM04CD150J03
C14	Capacitor, 5 pf, Sil. Mica		CM04CD050D03
C5	Capacitor, Sil. Mica		Select

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 TRANSMITTER (ECL) P.C. BOARD ASSEMBLY (Con't)			
U18	Integrated Circuit	Motorola, Fairchild or Signetics	MC10116P or F10116PC
U20	Integrated Circuit	Motorola, Fairchild or Signetics	MC10103P or F10103PC
U23	Integrated Circuit	Motorola, Fairchild or Signetics	MC10106P or F10106PC
U29	Integrated Circuit	Motorola, Fairchild or Signetics	F10010PC
L3, 4	Inductor Ferrite Bead	Ferronics	21-031-J
L2, 1	Inductor, .56uh	Lenox Fugle	NRO.56 5%
FT3 TRANSMITTER (TTL) P.C. BOARD ASSEMBLY			
TP1-7,G,G	Terminal	Cambion	2027-2
P1	Connector R. Angle Header	3M	3429-1002
P2	Connector Straight	3M	3429-2002
P3	Connector R. Angle 3 Pin	Amp	640389-3
R33	Resistor, 470, 1/4W, 5%		RCR07G471JS
R1,2,3,4,5,8,9,10, R12,13,14,15,16,21, R26,28,30,34	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R6,17,18,19,20,22, R23,24,25,29	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R7	Resistor, 3K, 1/4W, 5%		RCR07G302JS
R11	Resistor, 5.1M, 1/4W, 5%		RCR07G515JS
R27	Resistor, 1K, 1/10W, 1%		RN55C1001JS
C1	Capacitor, 1uf, 5%, 100V, Polycarbon	Siemens	32561-1-5-100
C39	Capacitor, 200pf, S.M.		CM04FD201J03
C3	Capacitor, 39pf, NPO, 5%		CM04ED390J03
C40	Capacitor, S.M., 100pf		CM04FD101G03
C5	Capacitor, 6.8uf, 25V		196D685X9025JA1
C6 - C32, C34 - C36, C38	Capacitor, .01uf, 50V	Unitrode	CGC103ZDZ
C33, C37	Capacitor, 10uf, 16V, EL	Capar	CAE-E10M16V
C4	Capacitor, 390pf		CM05FD391J03

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 TRANSMITTER (TTL) P.C. BOARD ASSEMBLY (Con't)			
R31	Resistor, 160, 1/4W, 5%		RCR07G161JS
R32	Resistor, 270, 1/4W, 5%		RCR07G271JS
Q1	Transistor		2N3904
X1	Crystal, 1.88 MHz	M-Tron (Bowmar P/N)	B6485
D1	Diode		1N4148
U1, U2	Integrated Circuit	Motorola, Fairchild or Signetics	MC10124P or F10124PC
U3	Integrated Circuit	Motorola, Fairchild or Signetics	MC10125P or F10125PC
U4,11,12,13,18,24,29	Integrated Circuit		SN74161N
U5,8,7,19,20,23,27,30	Integrated Circuit		SN7400N
U6,10,15,26,28	Integrated Circuit		SN7474N
U9	Integrated Circuit		SN7486N
U14	Integrated Circuit	Motorola	MC14538BPC
U16, U21	Integrated Circuit		SN7404N
U17, U22	Integrated Circuit		SN74157N
U25, U31	Integrated Circuit		SN7410N
FT3 RECEIVER P.C. BOARD ASSMEBLY			
R142	Resistor, 4.75K, 1/8W, 1%		RN55C4751F
R144	Resistor, 3.65K, 1/8W, 1%		RN55C3651F
R36	Resistor, 75K, 1/8W, 1%		RN55C7502F
R102,103,122,130, R139,145,146,147, R149,150,153,154, R155,156	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R25,148,157	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R17,22,34	Resistor, 130, 1/4W, 5%		RCR07G131JS
R2	Resistor, 110, 1/4W, 5%		RCR07G111JS
R26,39,19	Resistor, 24, 1/4W, 5%		RCR07G240JS
R4,5,28,29	Resistor, 1.5K, 1/4W, 5%		RCR07G152JS
R16,24,41,185	Resistor, 3K, 1/4W, 5%		RCR07G302JS
R31	Resistor, 13K, 1/4W, 5%		RCR07G133JS
R32	Resistor, 510, 1/4W, 5%		RCR07G511JS
R186	Resistor, 51, 1/4W, 5%		RCR07G510JS
R187	Resistor, 20K, 1/4W, 5%		RCR07G203JS
R37	Resistor, 620, 1/4W, 5%		RCR07G621JS

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 RECEIVER P.C. BOARD ASSEMBLY (Con't)			
R3,38,48,49,50,51,52, R53,56,57,58,63,64,65, R66,67,72,73,75,76,77, R78,79,80,81,82,83,87, R88,89,90,91,94,97,106, R109,110,111,112,113, R120,121,124,125,126, R129,131,132,133,136, R140,141,182,183,184	Resistor, 470, 1/4W, 5%		RCR07G471JS
R14	Resistor, 1.5K, 1/10W, 1%		RN55C1501F
R15	Resistor, 38.3K, 1/10W, 1%		RN55C3832F
R18,23,35	Resistor, 180 ohm, 1/4W, 5%		RCR07G181JS
R84, 123	Resistor, 5.1K, 1/4W, 5%		RCR07G512JS
R33	Resistor, 1.33K, 1/10W, 1%		RN55C1331F
R151, R152	Resistor, 2.4M, 1/4W, 5%		RCR07G245JS
R6,11,13,20,27,40,8, R42,44,47,54,60, R62,69,71,85,93, R95,99,101,104, R108,115,117,119, R128,134,137	Resistor, 270, 1/4W, 5%		RCR07G271JS
R7,10,12,43,45,46,9, R55,59,61,68,70, R86,92,96,98,100, R105,107,114,116, R118,127, 135, 138	Resistor, 160, 1/4W, 5%		RCR07G161JS
R30	Resistor, 1.96K, 1/10W, 1%		RN55C1961F
R143	Resistor, Var., 5K	Helitrim	89W5K
C31, C35	Capacitor, 5%, 250V, .luf, Polycarbon	Seimens	B32561-.1-5-250
C34	Capacitor, 5%, 100V, luf, Polycarbon	Seimens	B32561-1-5-100
C6	Capacitor, 5%, 100V, .47uf, Polycarbon	Seimens	B32561-.47-5-100
C90	Capacitor, 220pf, Sil, Mica		CM04FD221J03

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 RECEIVER P.C. BOARD ASSEMBLY (Con't)			
C25	Capacitor, 100pf, Sil. Mica		CM04FD101G03
C2, C13	Capacitor, 15pf, Sil. Mica		CM04CD150J03
C8, C22	Capacitor, 150pf, Sil. Mica		CM04FD151J03
C12, 20, 27, 91	Capacitor, 33pf, Sil. Mica		CM04ED330J03
C18	Capacitor, 1000pf		CM06FD102J03
C11,16,17,23,24,26, C28,29,30,32,33,36, C19,C40-61, C63-88	Capacitor, .01uf, 50V	Unitrode	CGC103ZDZ
C1,3,4,5,7,21,92	Capacitor, .1uf, 50V	Unitrode	CGD104ZDZ
C9	Capacitor, 100pf, N08D, 5%	RMC	CM100N080-5%
C38, C39	Capacitor, 10uf, 16V, EL	Capar	CAE-E10M16V
C14	Capacitor, 27pf, 2% Sic. Mica	RMC	CM04ED270G03
C15	Capacitor, 2-8pf, Var.	Erie	DV11PS8A
C10	Capacitor, 7-25pf, Var.	Erie	DV11PS25B
C37	Capacitor, 6.8uf @ 6V	Sprague	196D685X9006HA1
Q2,3,4	Transistor		2N4209
Q1	Transistor		2N3904
D1, D2	Diode		1N4148
L1, 2	Inductor, 0.29uh, 2%	WECO	1564AG
U3, U26	Integrated Circuit	Motorola, Fairchild or Signetics	MC10125P or F10125PC
U27	Integrated Circuit	Motorola, Fairchild or Signetics	MC10124P or F10124PC
U1, U7	Integrated Circuit	Motorola, Fairchild or Signetics	MC10116P or F10116PC
U2,12,19,24	Integrated Circuit	Motorola, Fairchild or Signetics	MC10107P or F10107PC
U8,13,16,11,17,22, U25,31,33,34,38,39	Integrated Circuit	Motorola, Fairchild or Signetics	MC10231P or F10231PC
U15,18,23,37	Integrated Circuit	Motorola, Fairchild or Signetics	F10016PC
U20	Integrated Circuit	Motorola, Fairchild or Signetics	MC10176P or F10176PC
U14	Integrated Circuit	Motorola, Fairchild or Signetics	MC10103P or F10103PC
U9,10,42	Integrated Circuit	Motorola, Fairchild or Signetics	MC10102P or F10102PC
L3, 4	Inductor Ferrite Bead	Ferronics	21-031-J

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FT3 RECEIVER P.C. BOARD ASSEMBLY (Con't)			
U21, U32	Integrated Circuit	Motorola, Fairchild or Signetics	MC10106P F10106PC
U6	Op-Amp I.C.	Fairchild	UA741TC
U5	Tone Decoder I.C.	WECO	502ER
U4	Phase Lock Loop I.C.	WECO	555R LM555CN
U48	Timer I.C.		
U28, U51	Integrated Circuit		SN7410N
U29,43,50,59,64	Integrated Circuit		SN74161N
U30,53,56,60	Integrated Circuit		SN7490AN
U36,44,45,49,52, U55,57,61,63	Integrated Circuit		SN7474N
U35,40,41,46,47, U58,62	Integrated Circuit		SN7400N
U54	Multivibrator	Motorola	MC14538BPC
POWER SUPPLY ASSEMBLY PCB			
CR3, CR4	Diode		1N4720
C3,4,5,6	Capacitor, 2.2uf, 35V, Tant.	Sprague	196D225X9035JA1
R1	Resistor, 3.01K, 1/8W, 1%		RN60C3011F
R2	Resistor, 2.21K, 1/8W, 1%		RN60C2211F
MAIN ASSEMBLY FT3			
W1	Cable (Flat)	Bowmar	LMFT3-209
W2	Cable (Flat)	Bowmar	LMFT3-210
W3	Cable (Flat)	Bowmar	LMFT3-211
W4	Power Cable Assembly	Bowmar	LMFT3-208
FT3 POWER SUPPLY ASSEMBLY			
C1	Capacitor, 9400uf, 15V	Mepco/Electra	3120BA942U015AM
C2	Capacitor, 51,000uf, 15V	Mepco/Electra	3120EE513U015AM
VR1	Regulator	Fairchild	UA78H05SC
CR1, CR2	Diode		1N2794
VR2	Regulator	Fairchild	79BGKC

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FRONT PANEL ASSEMBLY FT3			
	Receptacle	Switchcraft	EAC-302
	3AG Fuse Extractor Post	Littlefuse	342014
	3AG Slo-Blo Fuse 1A	Littlefuse	315001
	Illuminated Rocker Switch	C & K	5201Q With Black (2) Bezel
	Thumbwheel Switch	Digitran	29102-1
	Thumbwheel Switch	Digitran	29102-2
	Jack	Trompeter	J12-5T
	Bulb T-1 3/4 Miniature Screw Base (6v)	Chicago Miniature	342

ACCOPRESS®

25970	YELLOW
25971	BLACK
25972	LIGHT BLUE
25973	DARK BLUE
25974	LIGHT GRAY
25975	LIGHT GREEN
25976	DARK GREEN
25977	TANGERINE
25978	RED
25979	EXECUTIVE RED

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